Design Guidelines for 2.5-D Packages Featuring Organic Interposer With Bridges Embedded

Yangyang Lai, *Member, IEEE*, Atsushi Takahashi, and Seungbae Park, *Fellow, IEEE*

***Abstract*— The rapid advancement of artificial intelligence (AI) has propelled the demand for high-performance computing (HPC) systems capable of handling vast amounts of data. This necessitates improvements in data processing speed within system-on-chip (SoC) units and efficient data transmission between SoC and high-bandwidth memory (HBM). Advanced packaging solutions, particularly the silicon interposer and organic interposer, have emerged to address these challenges. This article delves into the thermo-mechanical performance of 2.5-D packages with an organic interposer, focusing on warpage management during fabrication and stress analysis induced by coefficient of thermal expansion (CTE) mismatches. The study employs finite element analysis (FEA) modeling to evaluate the impact of various factors on warpage behavior and stress levels. Parametric studies on material selection and interposer geometric design reveal crucial insights. Specifically, reducing bridge die and redistribution layer (RDL) thickness mitigates warpage at the controlled collapse chip connection (C4) level, albeit with adverse effects on BGA level warpage. Material selection significantly influences warpage behavior. Organic materials with higher CTE reduce the mismatch between the interposer and the substrate but it is adverse for the interconnection between chiplets and interposer. Moreover, stress analysis indicates the organic interposer's effectiveness in reducing interconnection stress compared to silicon interposers. This research contributes valuable insights into the design and optimization of advanced packages with bridges embedded in organic interposers, providing guidelines for material selection and geometric design to enhance reliability and functionality. The findings facilitate the development of advanced packaging solutions capable of meeting the demands of AI-driven applications in challenging operational environments.**

***Index Terms*— Bridge dies, organic interposer, silicon interposer, thermo-mechanical reliability, warpage control.**

I. Introduction

IN RECENT years, the rapid advancement of artificial intelligence (AI) has surged, driven by breakthroughs in big data learning and training. This surge has fueled the need for enhanced high-performance computing (HPC) systems capable of handling vast amounts of data. To meet these demands, improvements in both data processing speed within the system on chip (SoC) and data transmission between SoC and high-bandwidth memory (HBM) are imperative [1]. Efficient data processing hinges not only on the speed of SoC units but also on the seamless flow of data between die-to-die [2]. The evolution of advanced packaging has introduced novel solutions to address these challenges [3]. Among these innovations, the silicon interposer stands out for its ability to accommodate big chiplets areas and versatility in supporting passives and interconnects [4], [5]. To meet the continual need for expanding integration areas, advancements in photolithography stitching enabled silicon interposer scaling up to three times the reticle size [6]. While scaling up to four times the reticle size is possible, challenges in productivity, reliability, and yield arise, making it extremely demanding [7].

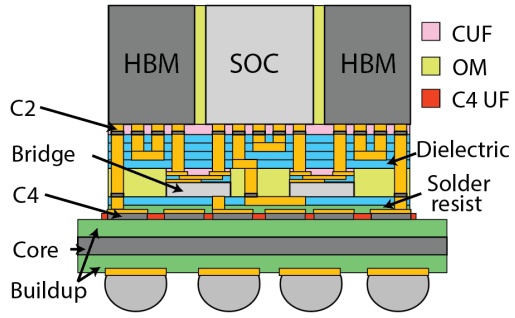

Fig. 1. Schematic of the 2.5-D package with organic interposer.

As shown in Fig. 1, the organic interposer utilizes the same assembly process as its silicon counterpart, with enhancements in yield and reliability. Copper traces and vias are constructed within a low-K polymer instead of silicon. An added benefit is the incorporation of redistribution layers (RDLs), which serve as a buffer to alleviate stress caused by coefficient of thermal expansion (CTE) mismatch between chiplets and substrate, leading to improved fatigue life of the controlled collapse chip connection (C4) joint [8]. This architecture allows for the embedding of silicon bridge chips into the interposer for die-to-die interconnects using a molding compound. Additionally, integrated passive devices can be integrated into the interposer as well to support its signal communication.

This article focuses on an in-depth examination of the thermo-mechanical performance of 2.5-D packages featuring organic interposers with bridges embedded. A critical aspect of this assessment involves analysis of the package warpage during both the packaging assembly process and thermal cycling or power cycling. The warpage management for different

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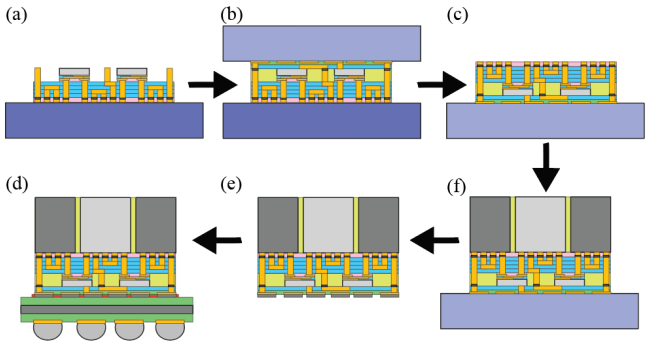

Fig. 2. Fabrication flow of 2.5-D package with organic interposer.

levels of assembling was thoroughly discussed. Additionally, the article also studies the stress induced by CTE mismatches, providing comparative insights across the spectrum of interposer design and material selections [9]. Stress analysis is indispensable for ensuring the reliability of interconnections and assessing the vulnerability to cracks and delamination at the interfaces within the packaging structures [10], [11]. By comprehensively evaluating the thermo-mechanical characteristics of these factors, this research contributes valuable insights to the field of advanced packaging solutions. Such insights are indispensable for the design and development of high-performance semiconductor packages, ensuring their reliability and functionality in the face of demanding operational environments.

The process flow for fabricating a 2.5-D package with an organic interposer is illustrated in Fig. 2. Initially, fine-pitch RDL, Cu pillars, and bridge chips are fabricated on the carrier wafer. Subsequently, the interposer is molded, followed by grinding and bottom RDL fabrication. Another carrier is then affixed to the organic interposer, which is flipped, and the first carrier wafer is debonded, as shown in Fig. 2(b) and (c). In Fig. 2(d), known good dies are bonded to the interposer using capillary underfill (CUF) and then encapsulated with overmolding (OM) materials. Finally, in Fig. 2(e) and (f), the stack of chiplets and interposer are bonded to substrates after being debonded from the carrier wafer [12].

In this study, particular attention is given to managing warpages during the fabrication process. The temporary glass carrier serves as a dependable platform, ensuring optimal flatness and consistent bump coplanarity. However, upon debonding of the chiplets and interposer stack from the glass carrier, the warpage resulting from CTE mismatch among materials presents a significant challenge to progress in subsequent stages.

II. Modeling and Simulation

A. Package Design and Material Properties

In formulating a design guideline, as depicted in Fig. 3, a 65 × 65 mm 2.5-D package serves as the reference configuration. Six HBM and a SoC are positioned on a 30 × 50 mm organic interposer, with six bridge dies facilitating connections between each HBM and the SoC. The silicon chiplets boast a thickness of 650 μm, while the interposer measures

TABLE I
Material Properties

	E (MPa)	CTE (PPM/C)	Poisson's ratio
Silicon	164000	3.2	0.22
Copper	121000	17	0.36
SAC 305	47500	23.56	0.35
Substrate Core	36000	4	0.3
Substrate Dielectric	13000	20	0.25
Solder Resist	4250	42.5	0.3
Interposer Dielectric-1	3500	65	0.2
Interposer Dielectric-2	9000	3	0.2
CUF-1	Fig. 4	27, 102 (Tg: 150°C)	0.25
OM-1	Fig. 5	7, 22 (Tg: 160°C)	0.25
CUF-2	Fig. 6	16, 62(Tg: 155°C)	0.25
MUF_1	Fig. 7	24, 43(Tg: 130°C)	0.25
OM-2	Fig. 8	13, 29(Tg: 155°C)	0.25

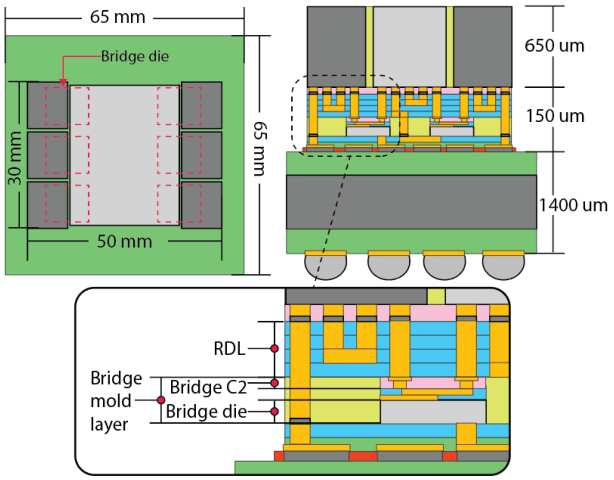

Fig. 3. General dimensions of the 2.5-D package.

150 μm in thickness. The substrate, with a thickness of 1400 μm, completes the structural composition. The chiplets are molded using OM. Both C2 and C4 interconnection layers are filled with CUF. General dimensions are provided solely for reference, while detailed specifications are withheld due to confidentiality concerns. The materials properties used in the modeling are listed in Table I.

B. Effective Material Properties

The 2.5-D package's structure can be regarded as a highly laminated composite. It is not practical to model all the

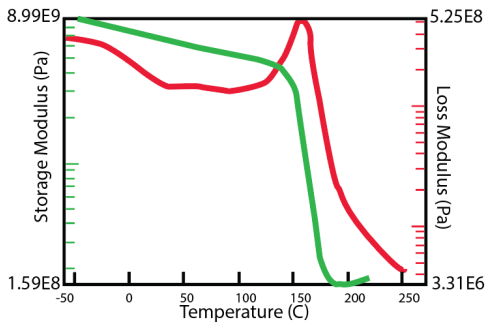

Fig. 4. Material characterization for CUF-1.

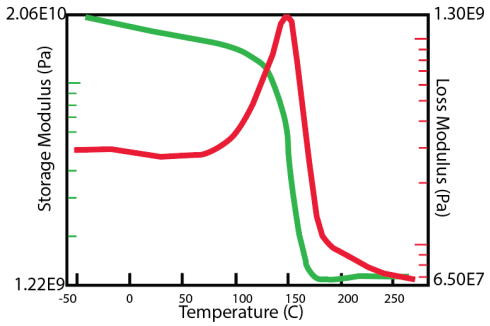

Fig. 5. Material characterization for OM-1.

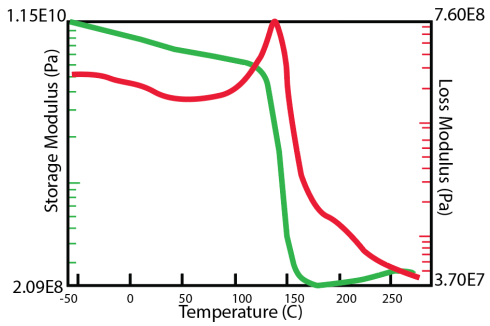

Fig. 6. Material characterization for CUF-2.

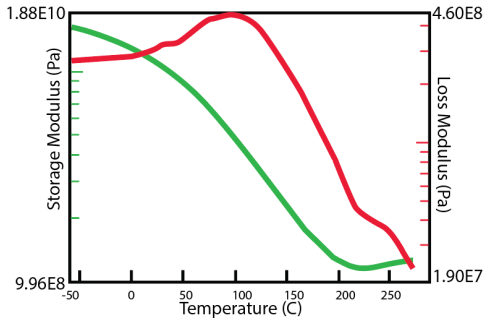

Fig. 7. Material characterization for MUF-1.

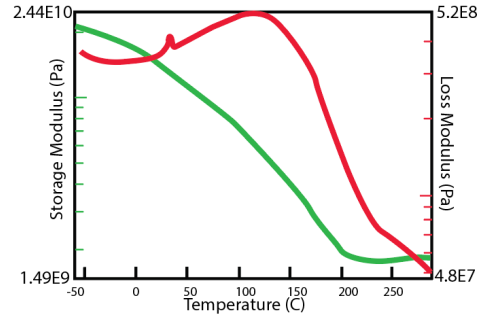

Fig. 8. Material characterization for OM-2.

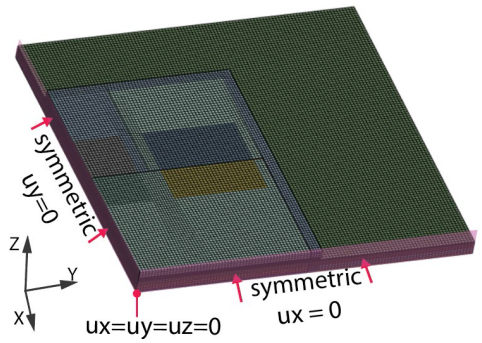

Fig. 9. FEA model and boundary conditions.

detailed structures in the finite element analysis (FEA) modeling. To simplify the model for the efficiency of computation, the effective material properties of interposer RDL, substrate buildup layer, underfilled C2 and C4 layers are calculated using the rule of the mixture as shown in (1)–(5) below [13]. These laminates are treated as isotropic layers and the in-plane effect material properties are used in the FEA modeling

$$E_{x,y} = \frac{1}{\left[\frac{C_s}{E_s} + \frac{C_u}{E_u}\right] - \frac{C_s C_u (v_s E_u - v_u E_s)^2}{E_s E_u (C_s E_s + C_u E_u)}} \tag{1}$$

$$E_z = C_s E_s + C_u E_u \tag{2}$$

$$\alpha_{x,y} = (1+v_u)\alpha_u C_u + (1+v_s)\alpha_s C_s - \alpha_z v_{xz} \tag{3}$$

$$\alpha_z = \frac{E_s \alpha_s C_s + E_u \alpha_u C_u}{C_s E_s + C_u E_u} \tag{4}$$

$$v_{xz} = C_s v_s + C_u v_u \tag{5}$$

where x, y are x, y are transverse directions, z is longitudinal direction, E is modulus of elasticity, c is volume fraction, v is Poisson's Ratio, α is CTE, s is copper or solder material, and u is organic material.

C. FEA Modeling and Boundary Conditions

To save the simulation efficiency, a quarter-symmetric 3-D finite element model with the appropriate boundary conditions was built using ANSYS-Mechanical as shown in Fig. 9. The reference temperature is assumed to be 150 °C, which corresponds to the approximate curing temperature of the epoxy. Note that any deviation in the reference temperature does not affect the trend of the results, as the differential CTE remains consistent. Thermal loading scenarios are considered at both room temperature (25 °C) and soldering temperature (220 °C). The overall package warpages are shown in Figs. 10 and 11. Due to silicon's significantly lower CTE compared to organic materials, the warpage exhibits a "smiling face" shape at 220 °C and a "crying face" shape at 25 °C. This parametric study is conducted to establish a package design strategy during the early design stage. It is important to note

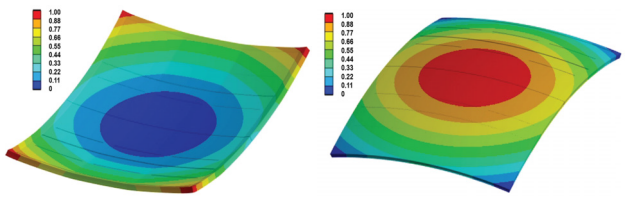

Fig. 10. Warpage of chiplets and interposer (a) at 220 °C and (b) at 25 °C.

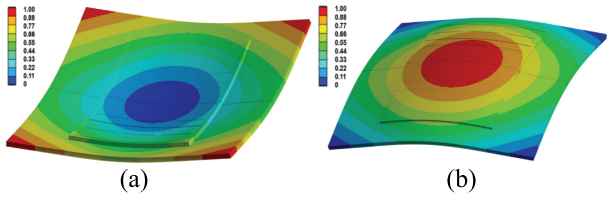

Fig. 11. Warpage of the entire package (a) at 220 °C and (b) at 25 °C.

TABLE II
PARAMETRIC STUDY OF CUF AND OM PROPERTIES

Group	M1	M2	M3
Bridge CUF	CUF-1	CUF-2	MUF-1
Bridge OM	OM-1	OM-2	MUF-1

TABLE III
PARAMETRIC STUDY OF INTERPOSER LAYER THICKNESS (μm)

Group	G1	G2	G3	G4	G5	G6	G7
Interposer RDL	42	28	28	28	42	42	42
Bridge C2	50	10	10	10	10	10	10
Bridge Die	25	50	65	105	50	65	105
Bridge Mold Layer	90	75	90	130	75	90	130

that the model has not undergone validation with physical samples at this stage. However, the demonstrated effectiveness of FEA in thermo-mechanical packaging simulation provides confidence in the study's applicability and insights.

D. Parametric Study Design

In this parametric study, both material selection and interposer geometric design are examined. Material properties of the bridge CUF and OM are selected as material factors as shown in Table II. Additionally, we designate the thicknesses of the interposer RDL, Bridge C2 layer, bridge die, and mold layer as geometric factors as shown in Table III.

The optimization aims to minimize warpage both at room temperature and soldering temperatures. Both the C4 level warpage, which occurs after separating the chiplets and interposer stack from the glass carrier, and the BGA level warpage, which occurs when the stack is bonded to the substrate, are examined in this study. For delamination risk and interconnection fatigue concerns, the maximum Von Mises stress and peeling stress in the underfilled C4 layers were also extracted from the FEA model results.

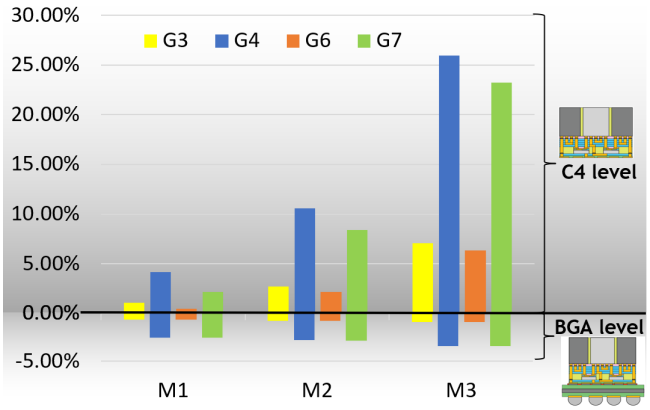

Fig. 12. Effect of bridge die thickness on warpage behavior.

III. RESULTS AND DISCUSSION

A. Parametric Study on Warpage

The influence of bridge die or bridge mold layer thickness is first analyzed as shown in Fig. 12. To mitigate the potential impact of interposer RDL thickness, G2 is designated as the reference group for G3 and G4, while G5 serves as the reference group for G6 and G7. The results reveal that while decreasing the thickness of the bridge die or bridge mold layer adversely affects warpage at the BGA level, the percentage improvement in warpage at the C4 level is notably higher. In the M3 group, the warpage at the C4 level with a 105 μm bridge die is more than 25% higher compared to that with a 50 μm bridge die.

The influence of the thickness of interposer RDL is shown in Fig. 13. To maintain RDL thickness as the only controlled variable, G2, G3, and G4 are considered as the reference group for G5, G6, and G7, respectively. It is observed that the thicker RDL induces a negative impact on warpage at the C4 level that is six–ten times greater than its positive impact at the BGA level. The comparison was based solely on warpages at room temperature, as their trend aligns with that observed at soldering temperature.

The effect of material selection on the warpage at the C4 level is shown in Fig. 14. The results of group M1 are taken as a reference. In group M2, the warpage at 220 °C shows better performance compared to that at 25 °C due to OM-2's considerably lower Young's modulus in comparison to OM-1, despite having a similar CTE after the glass transition temperature (Tg). In group M3, it is evident that MUF-1 has a substantial negative impact due to its significantly higher CTE. The warpage of M3 at 25 °C is notably worse than that at 220 °C, primarily because the difference in CTE before Tg between MUF-1 and OM materials in M1 and M2 is greater than the CTE difference after Tg.

The effect of material selection on warpage at BGA level is shown in Fig. 15 with M1 serving as the reference group.

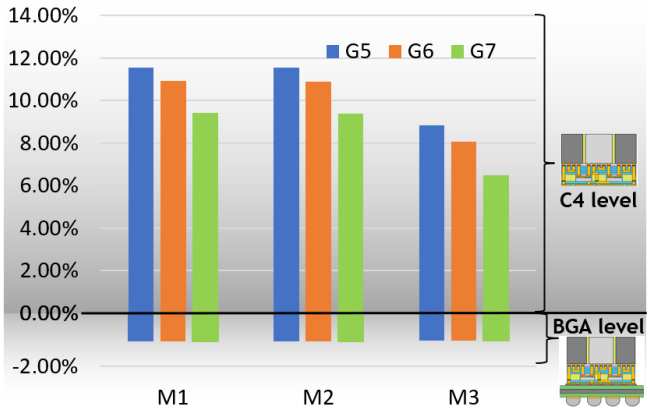

Fig. 13. Effect of interposer RDL thickness on warpage behavior.

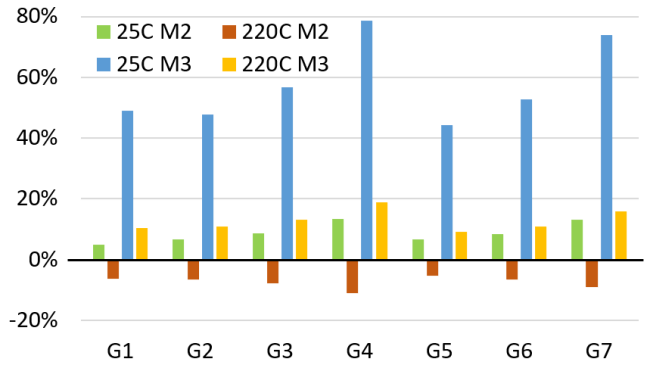

Fig. 14. Effect of material selection on warpage behavior at C4 level.

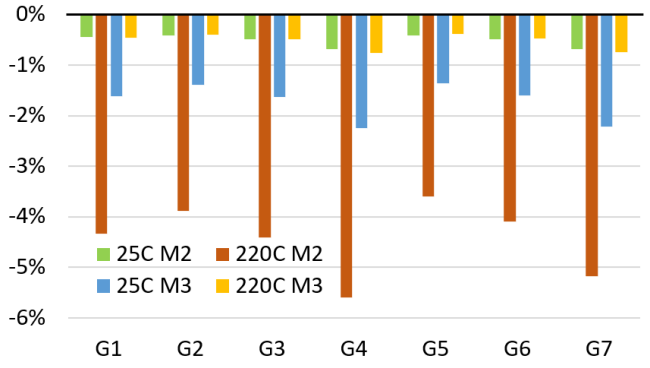

Fig. 15. Effect of material selection on warpage behavior at BGA level.

The influence on the BGA level is relatively minor compared to that on the C4 level, given that the interposer acts as a very thin component within the entire package structure.

The interposer serves as the central layer in the sandwich structure between the chiplets and the substrate within the entire package. At the C4 level, it functions like a bimetal structure with chiplets. At the BGA level, the stack of chiplets and interposers can be considered a consolidated unit in contrast to the substrate. Higher CTE and smaller Young's modulus contribute to a better balance with silicon chiplets and reduce the CTE mismatch between the consolidated unit and the substrate. This explains why the performance of M2 at 220 °C is superior to other cases. It is notable that the effect

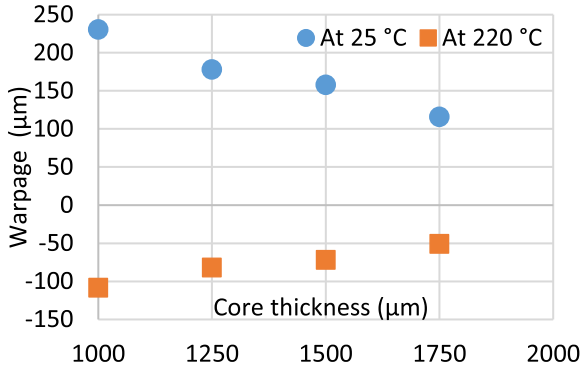

Fig. 16. Influence of the core thickness on warpage.

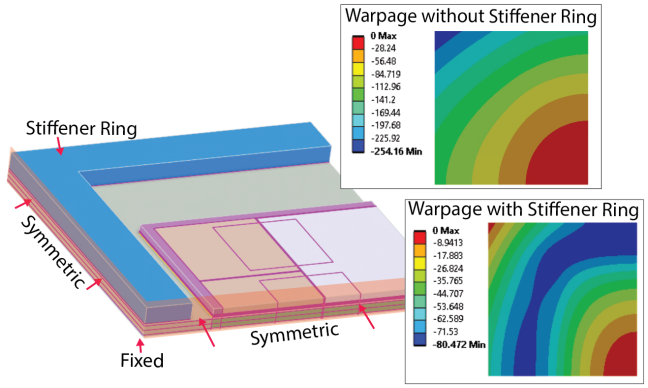

Fig. 17. Influence of the stiffener ring on warpage.

of the bridge OM material is greater than that of the bridge CUF material due to the difference in thickness.

Additionally, the impact of interposer dielectric materials was examined based on G1 and M1 settings. Dielectric-2 is a solid film material with a lower CTE and higher modulus compared to Dielectric-1. Employing Dielectric-2 resulted in a 46% reduction in warpage at the C4 level, while the warpage at the BGA level increased by less than 3%."

In this optimization process, we face a fundamental trade-off scenario where finding a perfect solution that effectively minimizes warpages at both levels proves to be mostly unattainable. Prioritizing efforts to reduce warpage at the C4 level is recommended, as alternative methods, such as increasing the substrate core thickness or implementing a stiffener ring, offer potential solutions for minimizing warpage at the BGA level. As depicted in Fig. 16, augmenting the thickness of the substrate core markedly diminishes the package warpage. Increasing the core thickness from 1000 to 1750 μm results in a 50% reduction in package warpage. As shown in Fig. 17, the inclusion of a copper stiffener ring results in a significant reduction of package warpage by 68%, transforming the warpage shape from a monotonic profile to a gull-wing shape.

B. *Parametric Study on Stress*

The maximum von Mises stress and peeling stress in the C4 layer, located at the corners of the molded chiplets, were extracted from the FEA modeling results. Fig. 18 illustrates the normalized stress values plotted alongside the normalized

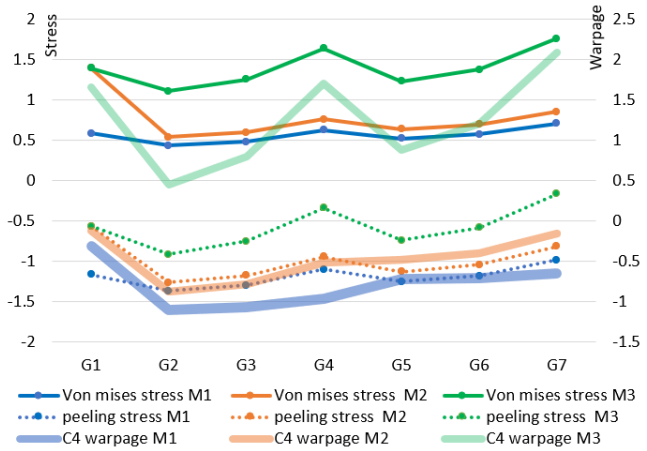

Fig. 18. Stress data and warpage data of C4 layer.

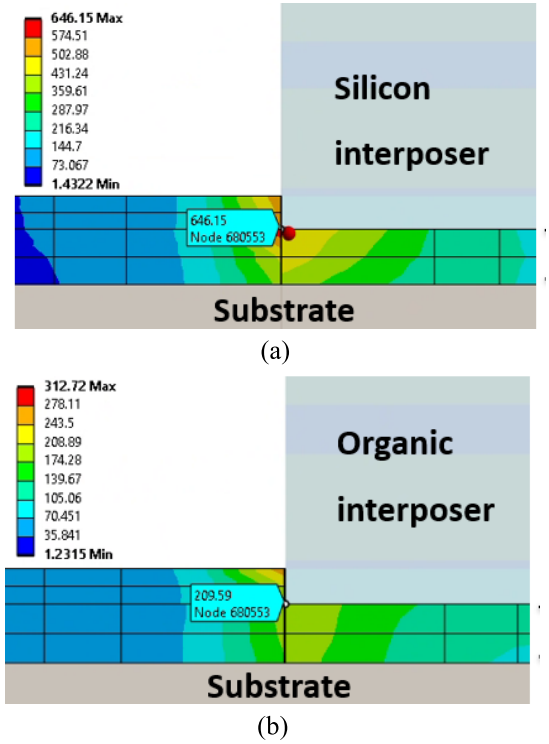

Fig. 19. Von Mises stress of C4 layer at the corner of chiplets (a) silicon interposer and (b) organic interposer.

warpage data, indicating a similar pattern between stress distribution and warpage in the C4 layer.

Furthermore, a comparative analysis was conducted between organic and silicon interposers to assess the effectiveness of the organic interposer's buffer effect in reducing interconnection stress. The geometric design and material selection were based on G1 and M1. Since stress singularities occurred in the FE modeling, the element shape and size were kept consistent to ensure a fair comparison. As shown in Fig. 19, a comparison of Von Mises stress in the C4 layer at the corners of chiplets reveals a 67% lower stress level in the organic interposer compared to the silicon interposer. The corner stress of the silicon interposer becomes a major concern when extending its size. However, comparing the interposer's corner stress with that of

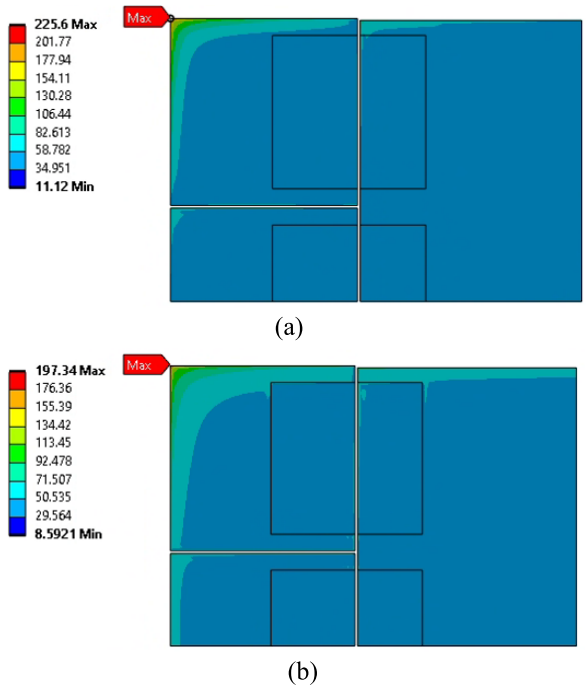

Fig. 20. Von Mises stress of C2 layer at the corner of chiplets (a) silicon interposer and (b) organic interposer.

an organic interposer was not conducted, as such a comparison between different materials may not yield significant insights.

Fig. 20 presents a comparison of Von Mises stress at the corners of chiplets in the C2 layer. Surprisingly, the stress in the silicon interposer is found to be higher than that in the organic interposer. The silicon interposer is believed to experience a minor CTE mismatch with silicon chiplets, which significantly alleviates stress in the C2 layer. However, upon assembly onto the substrate, packages with silicon interposers may exhibit more warpages than those with organic interposers due to the larger mismatch between the bulkier silicon stacks and the substrate. Meanwhile, the organic interposer serves as a buffer middle layer, absorbing certain levels of stress and providing benefits to both the C2 and C4 layers.

IV. Conclusion

This article has provided a comprehensive examination of the thermo-mechanical performance of 2.5-D packages with organic interposers, with a focus on managing package warpage and interconnection stress. Through analysis and simulation, it has been demonstrated that organic interposers offer several advantages, including improved stress absorption and better management of CTE mismatches compared to silicon interposers.

Parametric studies have shed light on the impact of material selection and geometric design on package warpage and stress analysis. Specifically, reducing bridge die and RDL thickness mitigates warpage at the C4 level, albeit with adverse effects on the BGA level warpage. Organic material with higher CTE reduces the mismatch between the interposer and the substrate but it is adverse for the interconnection between chiplets and interposer. While optimizing for minimal warpage

and stress at both the C2 and C4 layers simultaneously presents challenges, prioritizing efforts to reduce warpage at the C4 level is recommended. Innovative solutions such as incorporating copper stiffener rings have shown promising results in reducing package warpage. Furthermore, the comparison between organic and silicon interposers has revealed the beneficial buffer effect of organic interposers in reducing interconnection stress, despite potential CTE mismatches. This underscores the importance of considering material properties and design factors in advanced packaging solutions.

In summary, this research contributes valuable insights into the design and development of high-performance packages with bridges embedded in organic interposers, providing guidance for optimizing thermo-mechanical performance and ensuring reliability in demanding operational environments. Further research in this area holds the potential to drive continued advancements in advanced packaging technologies, meeting the evolving needs of AI-driven computing systems.

Author Contributions

Yangyang Lai: modeling, data analysis, and writing.

Atsushi Takahashi: project supervision, and research planning.

Seungbae Park: resources, Supervision.

Declaration of Competing Interest

The authors declare no known competing financial interests or personal relationships that could have appeared to influence the work reported in this article.

Data Availability

The authors do not have permission to share data.

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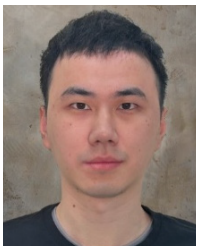

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