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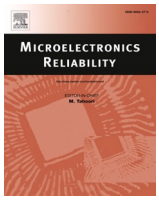

Review paper

Thermo-mechanical reliability of glass substrate and Through Glass Vias (TGV): A comprehensive review

Yangyang Lai *, Ke Pan, Seungbae Park

Mechanical Engineering, The State University of New York at Binghamton, Vestal, NY 13904, USA

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ABSTRACT

The evolution of electronic packaging technology towards the adoption of glass substrates marks a significant advancement in overcoming the constraints posed by traditional organic materials. This review delves into the thermo-mechanical reliability concerns associated with glass substrates, glass interposers, and Through Glass Vias (TGV), highlighting the inherent fragility of glass and its susceptibility to cracking as key challenges in their widespread application. The unique tunable modulus and closely matched coefficient of thermal expansion (CTE) to silicon, offer promising solutions to stress-related failures, particularly in large-format applications. Despite these advantages, the integration of glass substrates faces obstacles such as stress management, fragility, adhesion issues, and the uniformity of via fills, compounded by the limited availability of long-term reliability data. This paper provides a comprehensive overview of the fabrication processes for glass substrates and TGVs, the impact of design parameters such as via density and aspect ratio on glass substrate reliability, and the mitigation strategies for stress and crack of TGV. Through the examination of Finite Element Analysis (FEA) models and experimental data, we explore the delicate balance between the stress induced by Redistribution Layers (RDL) and the fracture strength of glass, influenced by various design factors. The review also considers the potential of glass substrates in high-density interconnects and advanced packaging architectures, positioning glass as a transformative material in the future of electronic packaging.

1. Introduction

In the evolving landscape of electronic packaging, the shift towards glass substrates represents a significant leap forward, offering enhanced capabilities and addressing the limitations of organic materials. The unique properties of glass substrates, such as their tunable modulus and coefficient of thermal expansion (CTE) closely mirroring that of silicon, play a pivotal role in minimizing stress induced by CTE mismatches, particularly in large form factor applications [1]. This compatibility ensures enhanced device reliability and longevity. Glass substrate further distinguishes itself through improved dimensional stability, enabling precise feature scaling as electronic devices shrink [2–4]. Their ability to support a higher density of vias, potentially tenfold that of organic substrates, facilitates complex circuit designs by improving routing and signaling [5,6]. Moreover, their low electrical loss enhances high-speed signaling, crucial for high-frequency applications [7–10]. The high-temperature resilience of glass substrates paves the way for advanced integrated power delivery systems, critical in high-power electronics [11]. The comparison between glass substrates and organic substrates is shown in Table 1 [12–17]. Despite replacing the organic core material, glass substrates with high-density TGVs have several potential applications including RF components [18,19], ultra-thin mobile device substrates [15,20], and 2.5/3D interposers of HPC [9,21–24], cavity-embedded devices [13,25–31], LiDAR's front end substrate [32], interposer with optical interconnects [33], Photonic MEMS [34].

Despite these advancements, the integration of glass substrates into mainstream applications faces significant hurdles. The challenges range from managing stress and handling fragility to overcoming issues with adhesion and achieving uniform via fills [35]. Moreover, the scarcity of long-term reliability data for glass, as compared to organic materials, raises concerns. The potential of glass substrates to support high-density interconnects essential for next-generation electronics is currently constrained by limitations in layering due to glass's brittle nature [36]. Additionally, the CTE differential between glass and other materials used in semiconductor devices introduces challenges during assembly, risking distortions and misalignments [37]. Despite these challenges, glass substrates bring distinct advantages, including the possibility of

* Corresponding author.
E-mail address: ylai9@binghamton.edu (Y. Lai).

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Table 1
Comparison between glass substrate and organic substrate.

	Glass substrate	Organic substrate
CTE	0–9 ppm/°C	3–17 ppm/°C
Young's modulus	50–90 GPa	10–40 GPa
Glass transition point	>600 °C	150–200 °C
Dielectric constant	~3–7	~4–8
Thermal stability	Excellent	Moderate
Transparency	Good for optoelectronic	No
Through-hole	Higher density	Lower density
	Smaller diameter	Larger diameter
Warpage	Lower	Higher
Cost	low in panel level	Lower
Manufacturing	Complex	Easier
Reliability	Higher for fine pitch	Lower for fine pitch
Moisture sensitivity	Lower	Higher

integrating novel inspection techniques due to their inherent transparency [38]. This could revolutionize quality control and device reliability assessment. As the industry navigates these complexities, the promise of glass substrates in enabling compact, high-performance packaging remains a compelling narrative, signaling a transformative phase in electronic packaging technology.

This review paper focuses on thermos-mechanical reliability challenges for glass substrates, and through glass via (TGV). TGVs, which are vertical interconnects embedded within glass substrates, enable high-density, multi-layered circuit integration by allowing electrical signals to pass through the glass. From a thermo-mechanical reliability perspective, this paper examines two main areas: the internal interaction between the glass and the copper vias (TGV reliability) and the interaction between the entire glass substrate and other layers, such as Redistribution Layers (RDL) or silicon dies (glass reliability). Additionally, the design and density of TGVs significantly influence the thermal and mechanical properties of the entire glass substrate [39]. This intricate linkage is critical for ensuring the overall reliability and performance of the electronic packaging system.

The fragile characteristics of glass, coupled with its low resistance to cracking might significantly impact the dependability of packaging systems that utilize glass interposers and substrates [39]. To produce a glass substrate, Redistribution Layers (RDL) are established by layering polymer and copper onto two sides of glass panels. Thermo-mechanical tensions arise due to the differential CTE among the RDL and glass in the fabrication process and during thermal cycling [40]. The number of RDL that can be applied to glass is still substantially restricted. Subsequently, glass panels require singulation into unit substrates via dicing, potentially introducing substantial defects that could initiate crack formation, ultimately resulting in the fracturing of the glass substrate [41]. For TGVs, reliability concerns encompass radial and circumferential glass cracking, copper protrusion, as well as delamination and sliding at the interface of glass and copper [42]. In addition to the thermal stress experienced during thermal cycling, an annealing process post-copper electroplating essentially alleviates the residual stress in the copper, potentially reaching up to 400 °C, thereby increasing the failure risk associated with TGVs [43].

2. Glass substrate fabrication process

The fabrication of glass substrates involves both the formation of TGVs and subsequent glass panel fabrication. Initially, TGVs are created within the glass cores to enable high-density vertical connections crucial for advanced electronic packaging. Following TGV formation, the glass panels undergo further processing steps, including the lamination of dielectric polymer layers and the formation of copper traces. Once all layers are fabricated, the glass panels are then segmented into unit substrates.

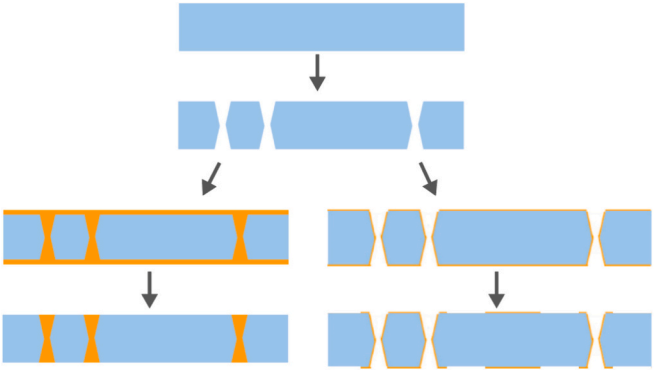

Fig. 1. TGV fabrication process for fully filled via and conformal plated via [44].

2.1. TGV formation process

The basic fabrication process of TGV is shown in Fig. 1 [44–46]. Glass vias can be made using ultrasonic drilling, ultrasonic high-speed drilling (USHD), sandblasting, mechanical drilling, chemical electrical discharge, and laser drilling [19,33,47,48]. Among these methods, laser drilling is the most commonly used technology, which includes CO2 laser, UV laser, and Excimer laser [14]. After the via formation, titanium or copper seed layers are deposited on the wafer surface via physical vapor deposition (PVD), with thicknesses of 300 nm for titanium and 500 nm for copper, ensuring continuous coverage via's center. Subsequent electroplating was complemented by an annealing step, which facilitated the growth of copper grains within the via and relieved stress. Excess copper is then eliminated using Chemical Mechanical Polishing (CMP). The annealing process may reach temperatures as high as 400 °C, subjecting the materials to a thermal load greater than that experienced during thermal cycling [49]. Shorey et al. proposed a temporary bonding technology as a solution for thin glass handling, aiming to circumvent the need for expensive back-grinding processes [50].

The author provides only a basic overview of the TGV formation. Given glass's brittle nature and the limitations involved in drilling, etching, seeding, and plating for various TGV designs, the industry is continuously optimizing the fabrication process.

2.2. Glass panel fabrication process

Fig. 2 shows a detailed fabrication process of glass panels [40,51–53]. Initially, the glass panel is coated with a dielectric polymer layer. To enhance the bond between the glass and polymer, a silane coupling agent is applied followed by dielectric curing. After that, the formation of copper traces was achieved with the application of an electroless copper seed layer. Following this, a dry film photoresist is affixed and subsequently undergoes exposure and development, paving the way for the electroplating of copper. After the removal of the photoresist and etching away the seed layer, a copper thickness between 3 and 10 μm remains. This layer then undergoes an annealing treatment. This process allows for the simultaneous formation of polymer and copper trace layers on both sides of the panel. Subsequent iterations of the dielectric polymer application and the semi-additive technique allow for the incorporation of more RDL layers on each side. To complete the process, a surface finish is applied to the copper pads. Additionally, a dry film passivation layer is affixed, exposed, developed, and cured.

Once all layers are fabricated, the glass panels are then segmented into quarter panels and subsequently diced into unit substrates. As shown in Fig. 3, The glass panels feature specific patterns with varying ratios of copper to dielectric material. The active unit area encompasses the substrate's unit design. Saw streets lack copper and are composed

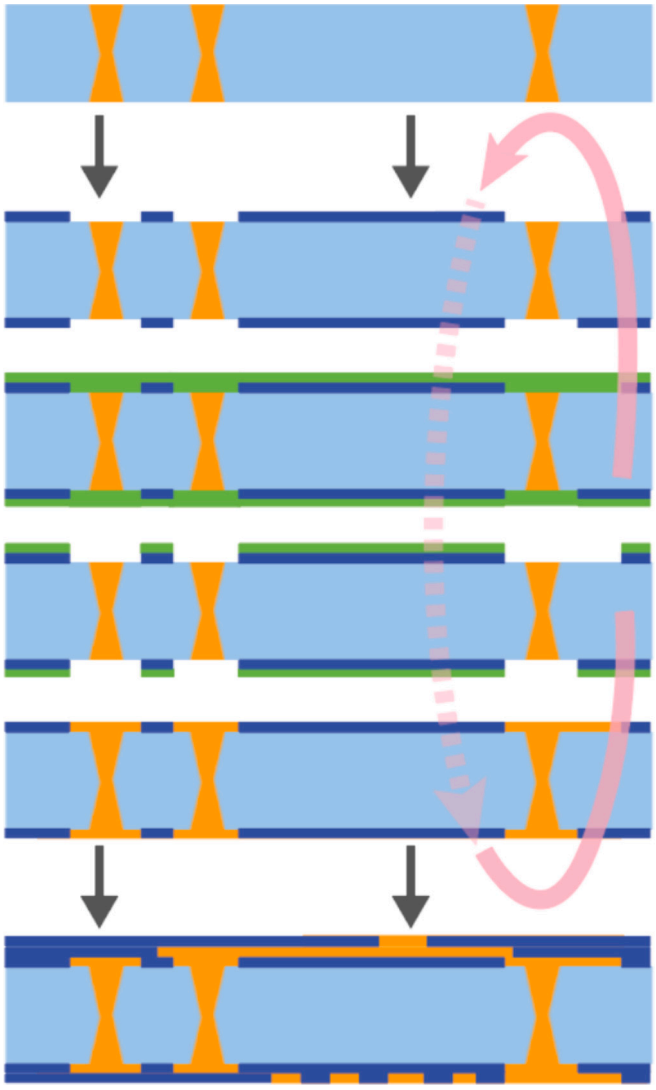

Fig. 2. Glass substrate fabrication process [40].

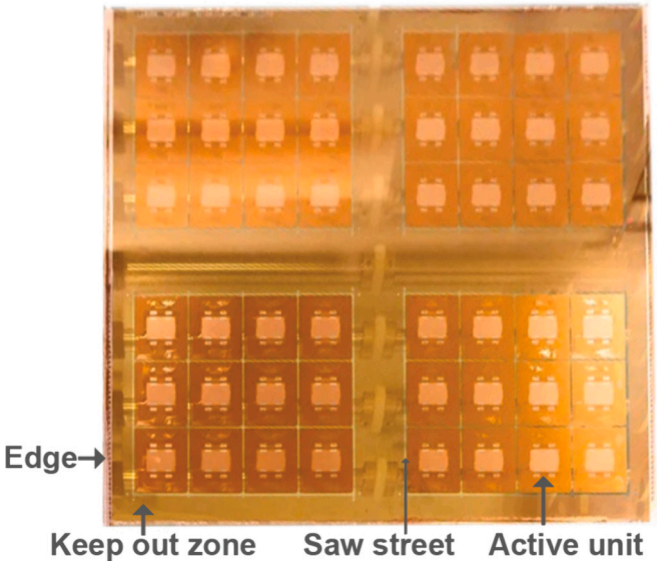

Fig. 3. Panel level glass substrate [54].

solely of dielectric material to facilitate dicing into quarter panels and individual units. The keep-out zone is designed with varying metal densities to counteract panel warping. The edge area predominantly comprises copper.

3. Thermo-mechanical reliability of glass substrate

This section covers the thermo-mechanical reliability of glass substrates, focusing on two key aspects: the reliability of the glass core caused by the interfacial stress with buildup layers, as well as concerns regarding the entire glass substrate's warpage and strength. The second aspect is the reliability of TGVs, which involves the interaction between glass and filled copper.

3.1. Glass core fracture

As shown in Fig. 4, basically there are three types of glass core cracking [55,56]. Cohesive glass cracking and interfacial delamination occurs during or shortly after dicing. The other type is a three-stage failure process begins with dicing-induced defects, followed by delamination at the interface between glass and RDL, culminating in the crack's propagation into the glass. Fig. 5 shows scanning electron microscopy images that capture the edge of a glass substrate post-crack propagation, respectively. The delamination between the glass core and buildup layers is not the main focus because the mechanism is similar to that of organic substrates, which can usually be improved by optimizing surface preparation and deposition techniques. The unique concern for glass is cohesive cracking, which is related to interface stress and defect control.

McCann et al. employed a 2D plane strain finite element analysis (FEA) model to examine how the thickness of the RDL and edge pullback design affect the energy release rate (ERR) at the crack tip resulting from substrate dicing [55]. Contour integral approach and Virtual Crack Closure Technique (VCCT) were used to evaluate the energy release rate at the crack tip (Fig. 6). Variations among the five sample types are detailed in Table 2. The comparison of 5 types of design is shown in Fig. 7. The energy release rate has been noted to be directly proportional to the size of the initial defect. Thinner dielectric and metal layers prove beneficial in reducing the energy release rate. Moreover, the influence of core thickness on crack propagation has also been studied [57]. The results show that thicker glass cores have slightly lower energy release rates than thinner ones. However, this comparison is highly dependent on the initial defect location. The closer the defect is to the interface between the RDL and the glass, the less dependent it is on the core thickness. Since the location of defects is not controllable, maximum principal stress should serve as an additional metric for assessing glass crack concerns.

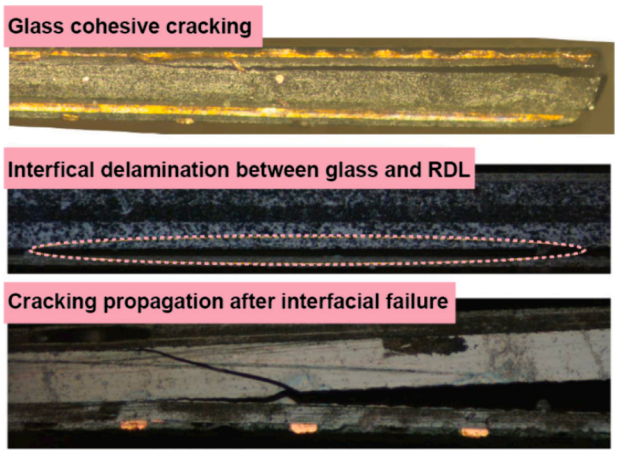

Fig. 4. Glass substrate cohesive crack and interfacial delamination [40,55].

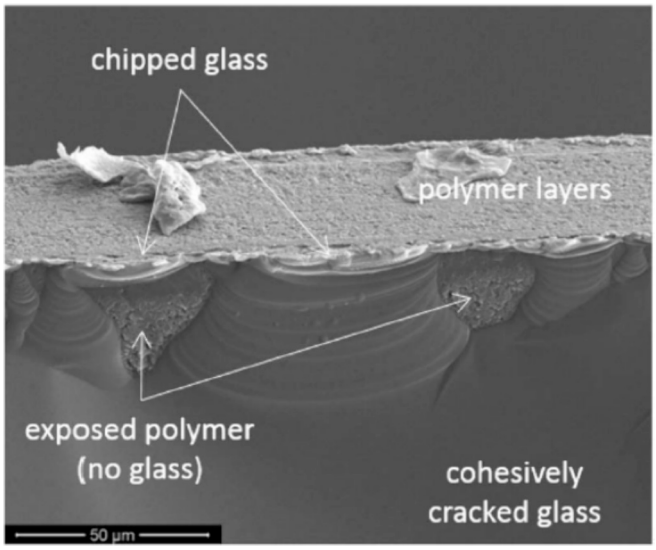

Fig. 5. SEM images of glass substrate edge after crack propagation, showing dicing induced defects, delamination, and cohesive cracking of the glass [55].

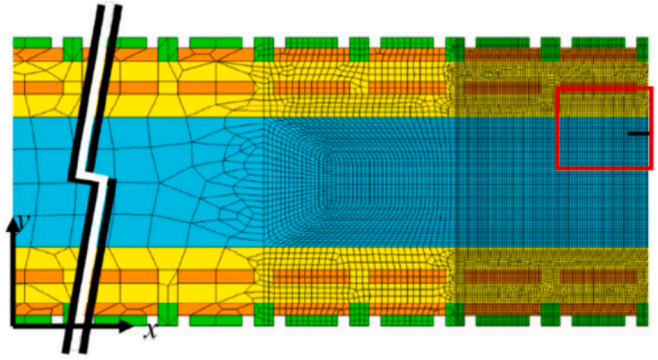

Fig. 6. FE model of glass substrate [55].

Table 2
Variations of five types of samples [55].

Batch	A	B	C	D	E
Dielectric thickness (um)	22.5	17.5	10	17.5	10
Copper thickness (um)	10	10	5	10	5
Glass core thickness (um)	100	100	100	100	100
Solder resist pullback (um)	N/A	N/A	N/A	150	150

There are limited studies addressing glass core fracture concerns, yet it remains one of the significant obstacles to applying more buildup layers on glass substrates. Additional research is required to investigate the impact of panel size on glass fractures [26]. This is crucial because CTE mismatch-induced stress is directly related to the Distance from Neutral Point (DNP), which is the linear distance measured from the center of the glass to the corner [58].

3.1.1. *The prevention of glass core fracture*

The pullback design in Table 2 aims to reduce the solder resist material's thickness near the free edge, thereby lessening the stress intensity in the vicinity of the crack tip as shown in Fig. 8(a). It mitigates the energy release rate, offering an effective prevention solution. Furthermore, edge coating was used to create a protective polymer layer on the diced edge of the glass substrate as shown in Fig. 8(b). This coating compresses the glass post-dicing, thereby shielding it from

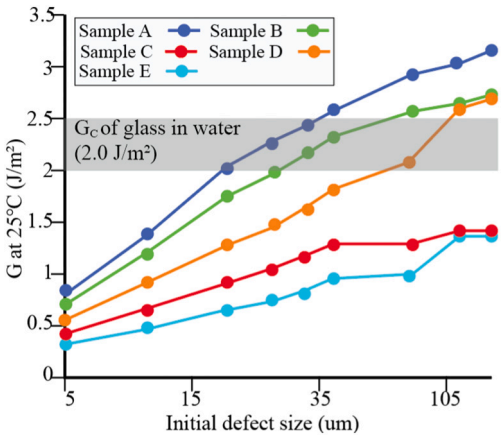

Fig. 7. ERR as a function of initial defect size [55].

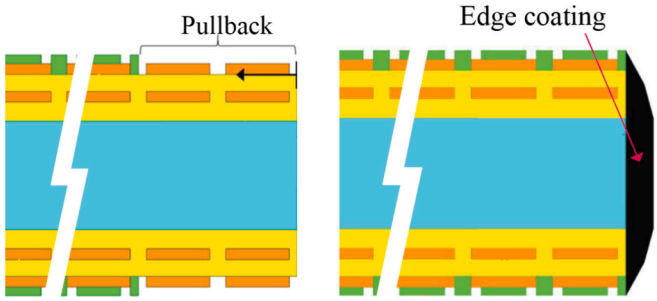

Fig. 8. Glass crack preventions (a) solder resist pullback [55], (b) edge coating [56].

moisture penetration, which in turn helps to prevent glass cracking due to RDL stresses and dicing defects. FEA modeling, as depicted in Fig. 9, was employed to quantitatively assess the impact of edge coating, demonstrating a significant reduction in stress due to the application of the coating.

The optimizations of dicing process were studied to prevent crack propagation [56]. Additionally, the double side processing was proposed to perform steps on both sides of the substrate simultaneously, rather than completing one full layer on top and then starting on the bottom layer [21,51]. By balancing the copper content in the buildup

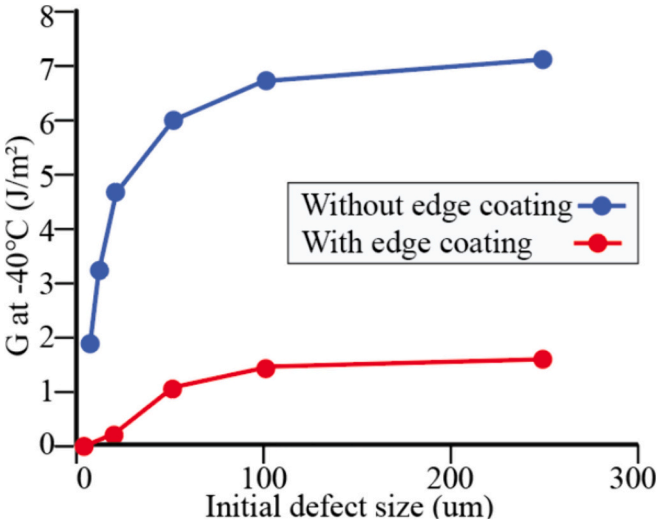

Fig. 9. The influence of edge coating ERR [56].

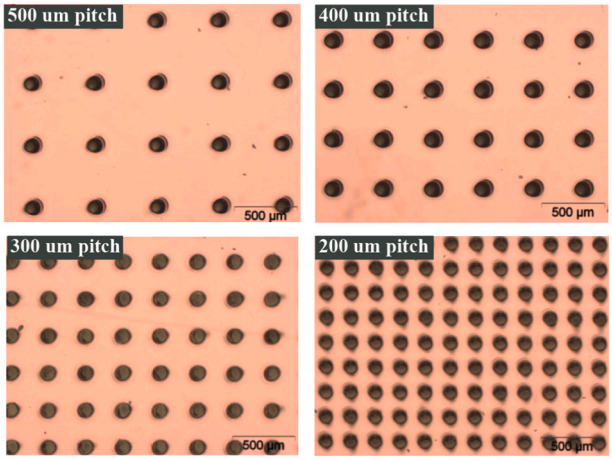

Fig. 10. Specimens with four kinds of TGV patches [39].

layers on each side, substrate warpage can be minimized. However, reduced warpage does not necessarily equate to lower interfacial stress. It simply indicates a more balanced stress distribution on each side of the sandwich structure.

3.1.2. The interaction between glass strength and TGV density

TSMC published their research on how the density of copper vias affects the fracture strength of glass substrates [39]. 4 point bending test was conducted for multiple specimens with four kinds of TGV pitches as shown in Fig. 10. As shown in Fig. 11, it was found that fracture strength diminishes as via pitch decreases, attributed to an increase via density resulting in a reduced cross-sectional area, thereby lowering observed strength.

As we know, crack propagation at the glass core's edge is closely related to stress induced by CTE mismatch. Given that the glass's CTE is typically tuned between 0 and 6 ppm/°C, and copper's CTE stands at 17 ppm/°C, the effective CTE of glass core with higher TGV density can significantly reduce the CTE mismatch between the RDLs and the glass core, thereby reducing fracture risk. However, the results in this section show that TGV density negatively impacts glass strength, serving as a metric for failure caused by substrate warpage. Balancing the RDLs on each side to reduce substrate warpage might be an effective solution to address this tradeoff.

This tradeoff becomes more complex when considering the interaction between silicon dies and the entire substrate. The introduction of glass material aims to match its CTE more closely to that of silicon dies. With a higher TGV density, the effective CTE of the glass core would deviate further from that of silicon. In the later sections, the influence of TGV pitch on TGV internal failure will be discussed, providing another dimension of concern regarding TGV density's impact.

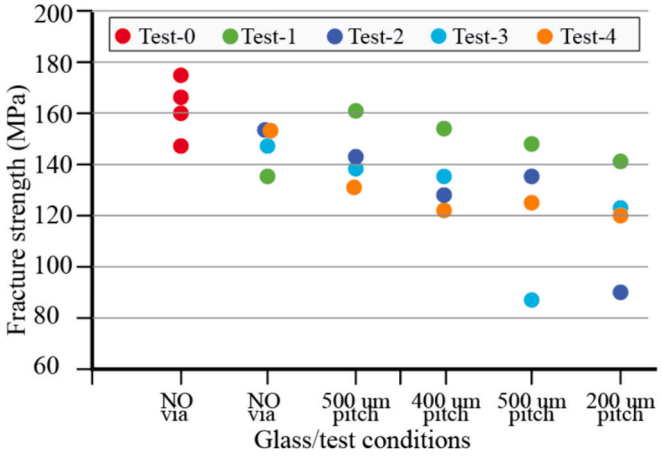

Fig. 11. The influence of TGV pitch on glass strength [39].

3.1.3. Glass substrate reliability at board level and wafer package level

As shown in Fig. 12, a board level simulation was conducted to study the influence of many design factors including die thickness, glass thickness, glass CTE, via diameter, via pitch, and solder material (eutectic and lead-free). Fig. 13 reveals that the maximum principal stress within a glass substrate is predominantly influenced by the thickness of the silicon die. Other factors exert less impact by comparison. A glass substrate with a moderate CTE, approximately 8.3 ppm/°C, experiences less stress due to minimized CTE mismatches with both the die and PCB, thus easing thermo-mechanical stresses. Fracture strength, as determined by four-point bending tests on glass with embedded vias, ranges between 120 and 140 MPa. Meanwhile, simulation findings indicate potential stress levels in glass between 80 and 100 MPa, approaching the material's fracture limit. This analysis highlights the critical need for stress mitigation and fracture strength improvement in glass substrates, achievable via strategic optimization of package architecture and material selection.

ASE used FEA modeling to simulate an 8-inch glass wafer warpage behavior during assembly process as shown in Fig. 14 [2,59]. The Young's modulus and CTE of both glass and epoxy molding compound (EMC) are identified as design factors, each with three distinct levels. Fig. 15 illustrates how the maximum warpage varies with the CTE and modulus for 0.7 mm thick glass and an EMC structure with 0.7 mm thick and CTE of 10 ppm/°C. The warpage is observed to decrease with an increase in glass CTE, attributed to the reduced CTE mismatch between the glass and EMC. However, the variation in glass modulus, ranging from 69 GPa to 75 GPa, does not significantly impact the warpage performance. The findings presented in Fig. 16 indicate that the warpage is affected by both the modulus and the CTE of EMC. It is clear that warpage escalates with an increase in EMC's CTE. Conversely, a lower EMC modulus contributes to reduced warpage, owing to diminished flexural rigidity. It is found that both stress and warpage are used to study CTE mismatch between glass and other materials. It's important to note that the level of the warpage does not necessarily correspond to the

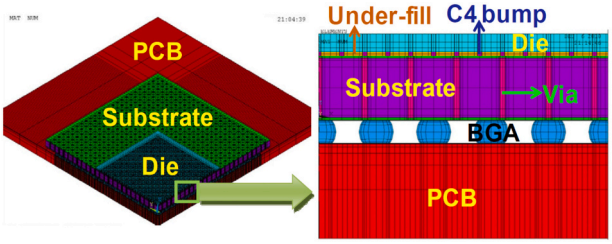

Fig. 12. FE modeling of glass substrate package [39].

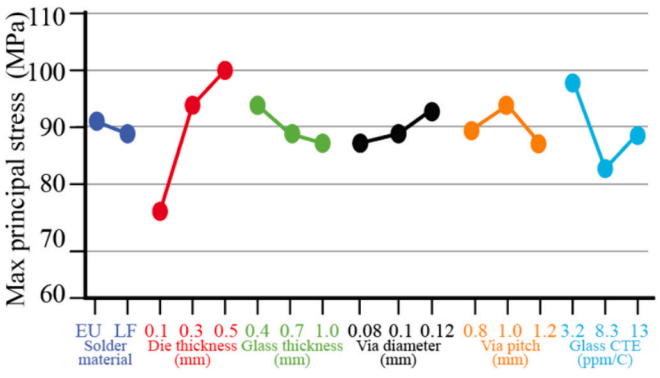

Fig. 13. Parametric effects on the maximum principle stress of glass [39].

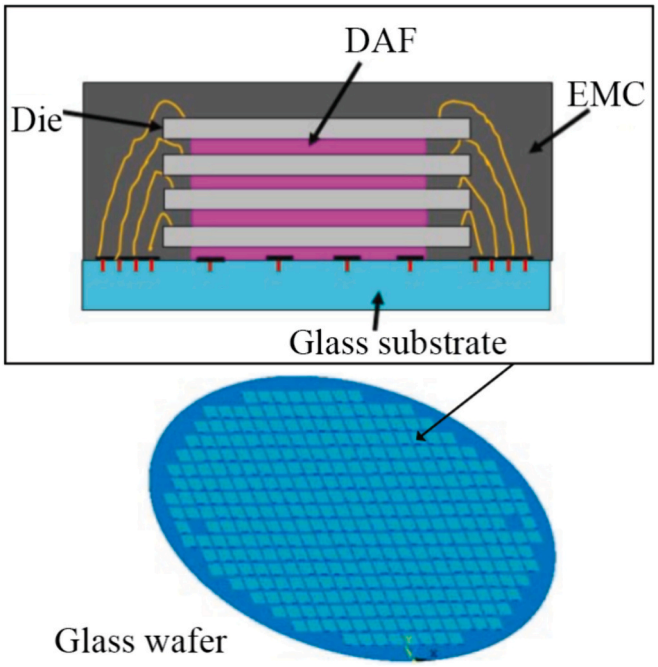

Fig. 14. Wafer level finite-element model of stacked BGA with glass substrate [59].

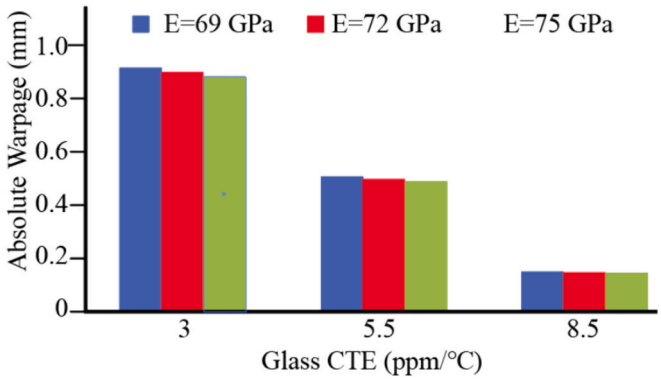

Fig. 15. Variation of maximum warpage with glass's CTE for various glass modulus [59].

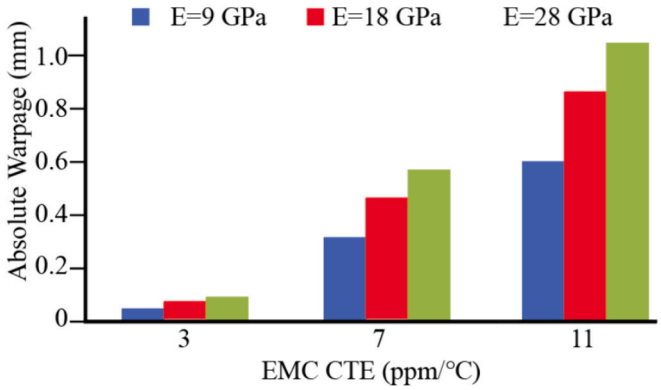

Fig. 16. Variation of maximum warpage with EMC's CTE for various EMC modulus [59].

level of stress.

The tunable properties of glass materials are a key motivation for the development of glass substrate technology. However, there is still no clear recommendation regarding the CTE strategy for glass. At the package level, the glass substrate and silicon die function like a bimetal structure. At the board level, the glass substrate serves as the middle layer in a sandwich structure between the PCB and silicon dies. The author believes this explains why a monotonic trend of glass's CTE is observed at the package level, while a sweet spot exists at the board level. Another study offers a similar recommendation, emphasizing that when selecting the CTE of a glass substrate, both chip-level and board-level fatigue life should be considered. This is because the CTE of the glass substrate has inconsistent influences at these two levels [60].

Due to the brittle nature of glass, the number of buildup layers that can be applied to glass is still limited [12]. The industry is actively seeking ways to route more connections through fewer layers or to develop new fabrication methods that allow for internal layering without compromising the substrate's integrity. Additionally, due to the scarcity of chip level reliability data, there is a need for further investigation into accelerated life testing of glass substrates and the development of predictive models for their long-term behavior under stress. The stresses introduced during manufacturing processes, such as dicing and handling of glass substrates, also require further study [36].

3.2. *Thermo-mechanical reliability of TGV*

Similar to the concerns associated with Through-Silicon Vias (TSVs), the reliability of TGV is primarily due to the CTE mismatch between the glass substrate and the filled copper. Silicon and glass are highly brittle materials, and it was shown that glass exhibits better and more consistent performance in terms of fracture strength [53,61]. However, the application of TSV and TGV technologies warrants further assessment of TGV reliability. TSV technology is mainly used in silicon dies and interposers, while TGV technology is intended for chip substrates, potentially replacing organic core materials. Consequently, the diameter of TGVs is typically larger than that of TSVs, which are usually $<$20 μm [42]. The interfacial stress is proportional to the via size, making the larger TGVs more susceptible to stress-related issues. Therefore, it is crucial to thoroughly evaluate TGV reliability to ensure the robustness of glass substrates.

Different from TSV crack failure, which primarily occurs along the crystallographic planes, two types of cracks may occur as shown in Fig. 17 [46]. Radial cracks develop during the heating phase as the copper exerts pressure on the glass substrate, leading to significant tensile circumferential stresses near the TGVs. The other type, known as circumferential cracks, emerges during the cooling phase when the contracting Cu tries to detach from the substrate. However, the strong adhesion between Cu and the substrate prevents this, causing substantial tensile radial stresses within the glass substrate. The optical microscopy images of the two types of cracks are shown in Fig. 18. It was shown that circumferential cracks are more dangerous than radial cracks [62,63]. However, this explanation is not entirely solid, as it primarily considers

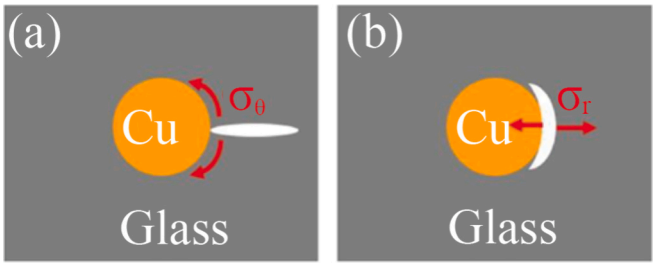

Fig. 17. Glass crack formation schematics (a) radial crack (b) circumferential cracks [49].

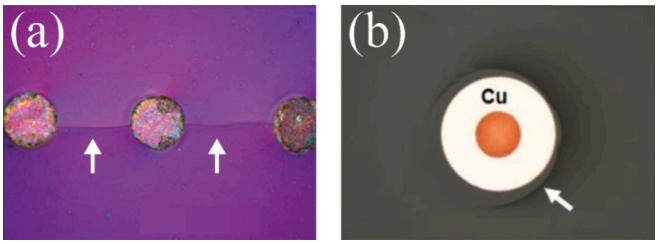

Fig. 18. Optical microscopy images of Cu TGV crack (a) radial crack [49] (b) circumferential cracks [64].

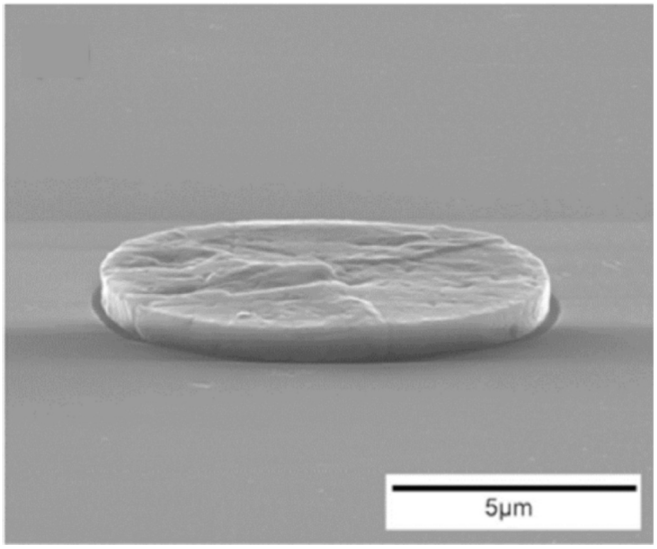

Fig. 19. SEM image of copper protrusion [65].

the risk of delamination for comparison. The copper protrusion as an inelastic out-of-plan deformation is also a significant reliability concern as shown in Fig. 19.

3.2.1. TGV reliability tests

Corning identified the thickness of the copper metallization at the conformally plated TGV as a pivotal factor in preventing circumferential cracks [64]. The likelihood of circumferential crack formation escalated exponentially with the thickness of the TGV Cu metallization as shown in Fig. 20. Nonetheless, under the specific TGV configuration and conditions examined in this research, it was observed that when the Cu metallization thickness was maintained below 12 μm, no cracks appeared in the substrate. It's important to highlight that although this study successfully achieved a crack-free TGV with metallization thicknesses below 12 μm, alterations in this threshold are anticipated should there be variations in any key parameters. These include changes in the substrate material properties, annealing temperature, TGV geometry, Cu plating chemistry, and Cu grain size, among others.

Corning also examined how the rate of heating, varying between 2.9 °C/min and 26 °C/min, impacts the development of radial cracks [49]. The investigation revealed that the quantity of radial cracks formed escalated with higher heating rates as shown in Fig. 21. Nonetheless, at heating rates of 6.5 °C/min or lower, no cracks emerged, indicating the complete avoidance of radial cracks. The relationship between the likelihood of radial crack formation and the heating rate during annealing was observed to adhere to an exponential function. This is because many stress relaxation mechanisms are time-dependent, which mitigates the accumulation of stress in the copper, consequently lowering the stress levels in the glass and thereby decreasing the likelihood of crack formation.

Corning measured the protrusion height of copper against annealing

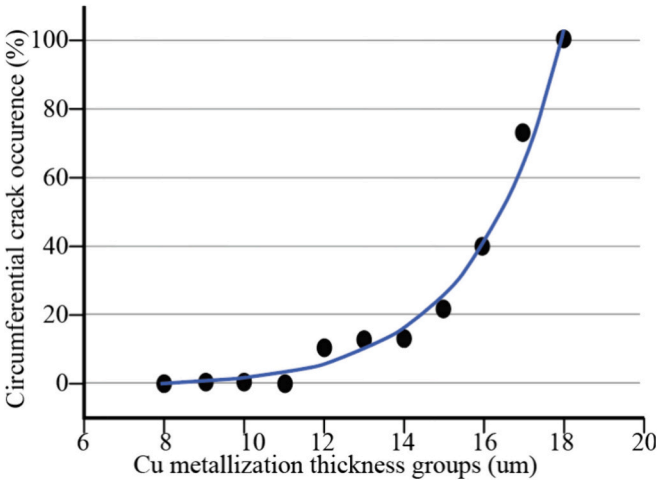

Fig. 20. Circumferential crack occurrence with respect to TGV Cu metallization thickness [64].

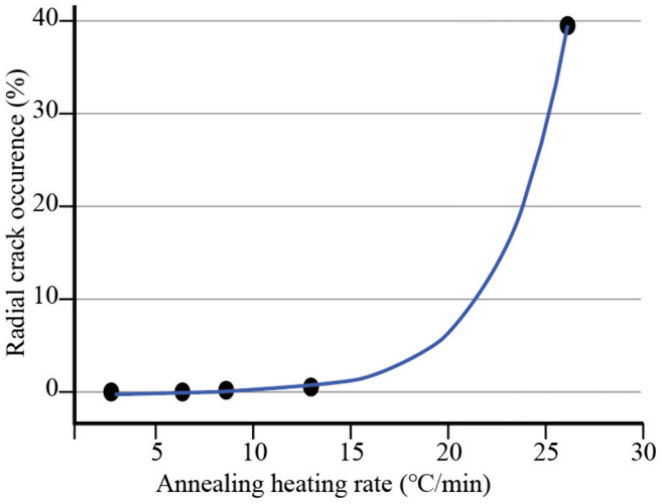

Fig. 21. Radial crack occurrence vs. annealing heating rate [49].

heating rates, finding that copper protrusion lessened with higher heating rates as shown in Fig. 22. It is found that Cu protrusion diminishes as the heating rate increases, indicating reduced stress relaxation at higher rates as shown in Fig. 23. Conversely, at lower heating rates, more pronounced Cu protrusion results in a smaller volume of Cu exerting force on the glass substrate. This reduction in force leads to lower stresses within the substrate, thereby decreasing the likelihood of radial crack development.

The impact of annealing dwell time was also examined, revealing that at a steady annealing temperature of 400 °C, Cu protrusion exhibits a dependency on the duration of the annealing process, reaching a saturation point approximately after 240 min as shown in Fig. 24. The annealing profile they used is a two-step process as shown in Fig. 25. It was found using an annealing dwell time of 120 min or longer resulted in no significant Cu protrusion in the second step. This suggests that extending the annealing dwell time to 120 min or more can prevent downstream Cu protrusion.

Additionally, a temperature-dependent analysis of the annealing process revealed that conducting the annealing at 450 °C for 60 min, followed by a thermal processing treatment at 400 °C for 60 min, effectively prevents downstream Cu protrusion. Thus, eliminating the second thermal processing treatment can be achieved either by prolonging the annealing dwell time to 120 min at 400 °C or by increasing

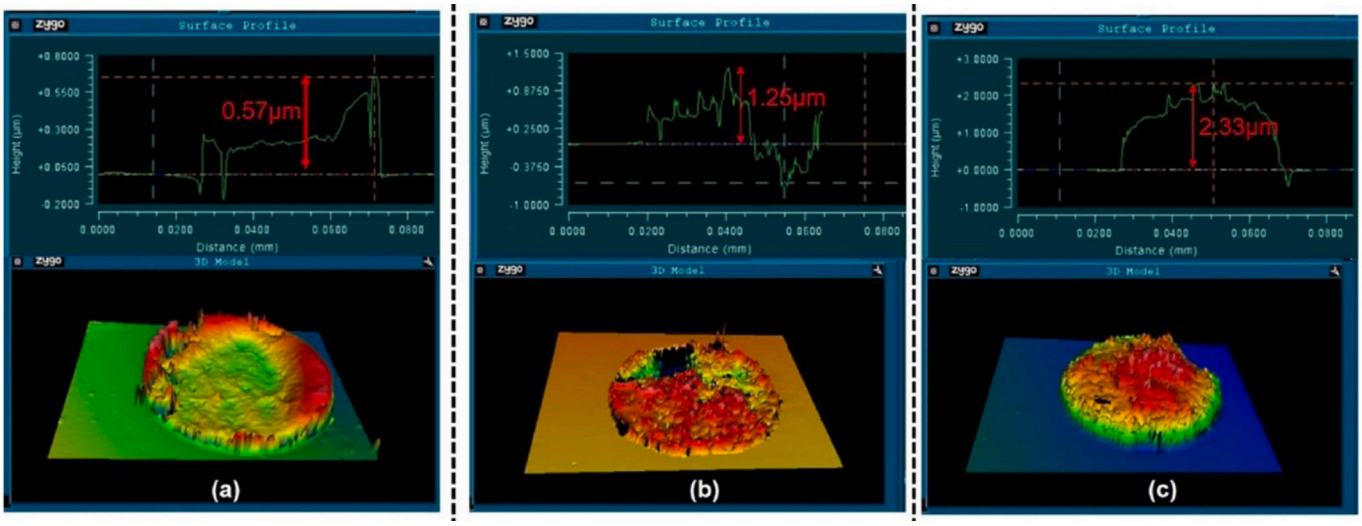

Fig. 22. Topography measurement of Cu protrusion height with respect to the applied heating rates (a) 26 °C/min (b) 13 °C/min (c) 6.5 °C/min [49].

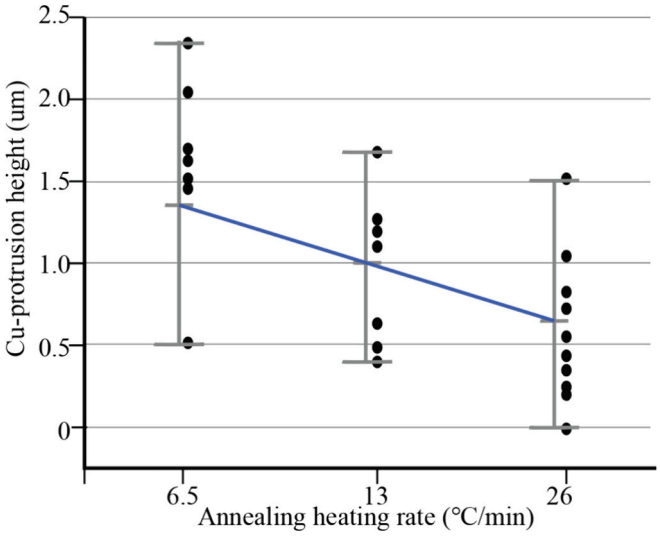

Fig. 23. Effect of annealing heating rate on copper protrusion [49].

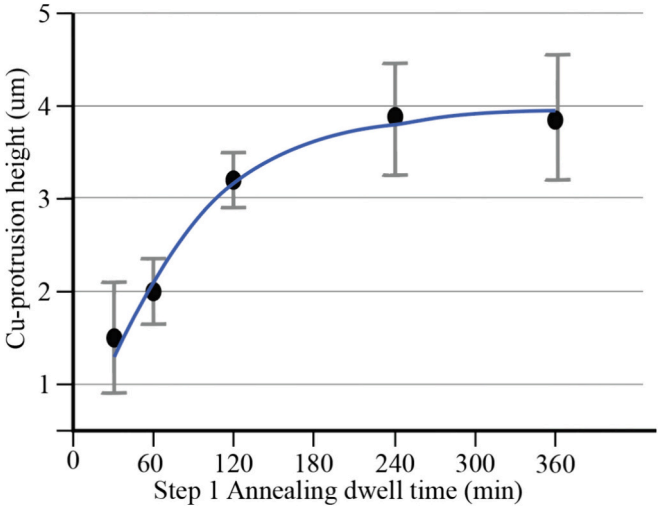

Fig. 24. Impact of annealing dwell time at 400 °C on Cu protrusion height [42].

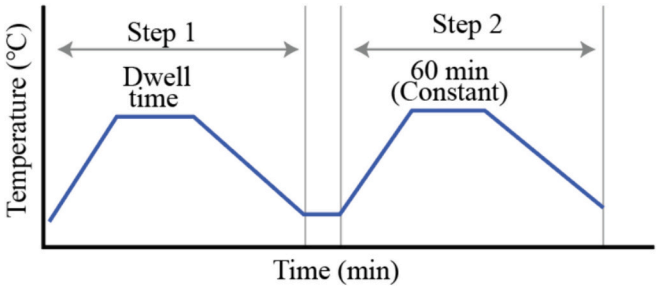

Fig. 25. Annealing temperature profile [42].

the annealing temperature to 450 °C with a 60-minute dwell time.

As mentioned in Section 3.2, the interfacial stress of TGVs is larger during the cooling phase than during heating [62,63]. However, there has yet to be a report on the optimization of the cooling profile, which is crucial for understanding the more often observed circumferential cracks in TGVs.

3.2.2. *Copper failures in TGV*

Most studies on TGVs focus on failures in brittle glass, with fewer reports addressing copper failures. Demir et al. conducted thermal cycling tests on fine-pitch glass interposers, subjecting them to temperatures ranging from −55 °C to 125 °C with a 15-minute dwell time [66]. Each tested specimen contained 64 vias, with each Through-Package Via (TPV) having a 60 μm diameter and a 120 μm pitch. The glass used in the interposers had a thickness of 180 μm, complemented by a 20 μm thick polymer liner. The criterion for failure was set at a 10 % deviation from the initial resistance value in the TPV daisy chain. Remarkably, 90 % of the test coupons passed after 1000 cycles, with

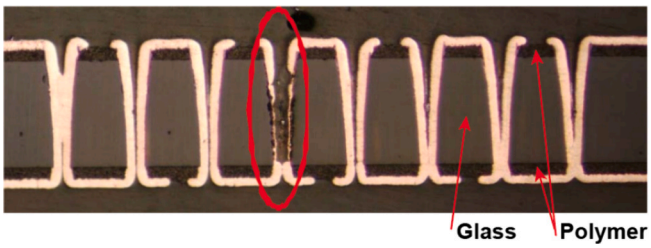

Fig. 26. Failed TPV after temperature cycling [66].

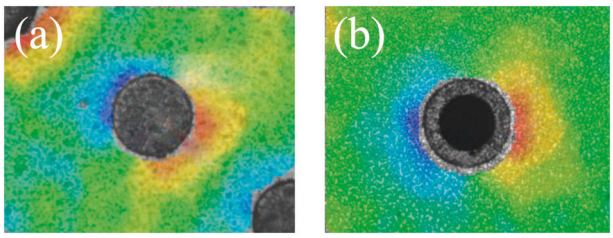

Fig. 27. Displacement of glass (a) fully filled TGV [35,69], (b) conformal plated TGV [43].

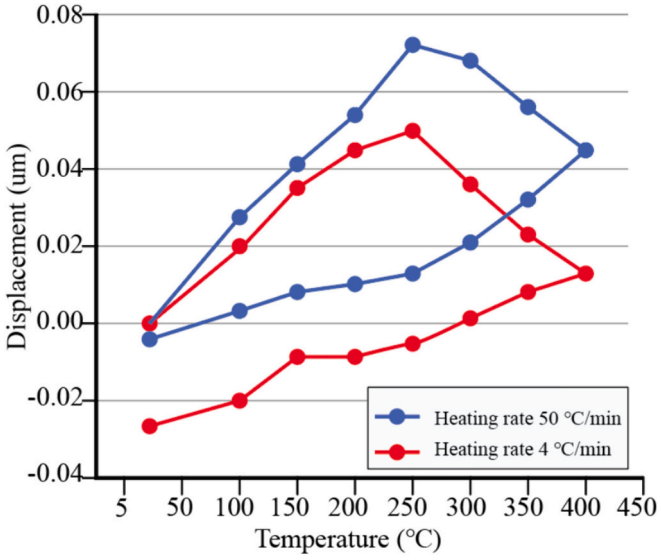

Fig. 28. Displacement of glass with 2 heating rates [43].

failures illustrated in Fig. 26. The primary cause of failure was identified as defects in the copper plating process, with particular challenges in plating high aspect ratio structures, leading to metallization issues in both individual TPVs and TPV arrays. Five years after their initial findings, Demir et al. reported observing neither visible degradation nor brittle fracture crack growth after subjecting the samples to 4000 thermal cycles, leading to speculation that improvements in the plating process might have contributed to these results [67].

3.2.3. Copper's nonlinear property

The properties of glass are stable across varying temperatures; however, copper exhibits nonlinear behavior that is both temperature and time dependent. Pan et al. conducted an in-depth analysis to characterize the nonlinear properties of copper by measuring the deformation of TGVs at elevated temperatures using the 2D digital image correlation technique [35,43,68,69]. The real-time, in-plane deformation of both fully filled TGVs and conformally plated TGVs are depicted in Fig. 27.

As shown in Fig. 28, the study observed an increase in the displacement of the glass as the temperature rose from room temperature to 250 °C. Beyond this point, the displacement began to diminish due to copper protrusion and creep occurring at elevated temperatures. To better explain this observation, time time-hardening model was selected to govern the creep properties of copper:

$$\dot{\varepsilon}cr = c_1 \sigma^{c_2} t^{c_3} e^{-c4/T} \quad (1)$$

where $\dot{\varepsilon}cr$ is the creep strain rate (1/s), σ is stress (MPa), t is time (Sec), and T is the temperature (K). In subsequent numerical modeling, the Cohesive Zone Model (CZM) was employed. The criterion for interfacial sliding due to shear stress is denoted as σ_T. Experimental data with four

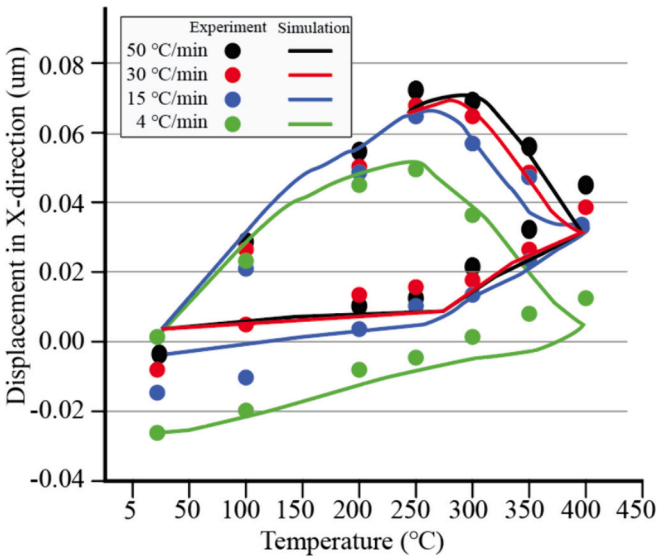

Fig. 29. Simulation results versus measurement results [43].

different heating rates were utilized to identify the optimal coefficients for the time hardening model, employing the root mean square error (RMSE) methodology to compare against simulation outcomes, as illustrated in Fig. 29.

3.2.4. Finite element analysis of TGV

Compared with limited testing data, FEA simulation is more widely used in parametric studies on TGV. A synthesis table is provided to summarize and compare the results of the published works (Table 3).

Ahmed et al. studied the interfacial delamination between glass and copper in a cooling process [63]. The combination of radial stress and shear stress promotes mixed mode (mode I and mode II) circumferential cracks (C-cracks) at the via/glass interface as shown in Fig. 30. By using FE modeling, the effect of via pitch, via design, glass property, aspect ratio and via metallization were studied.

There are two interesting observations that might challenge our first instincts. Fig. 31(a) indicates that positioning vias closer together is advantageous for TGV in minimizing the risk of interfacial delamination. Le and Choa reported similar observations in their paper [62]. This effect is attributed to the stress field generated by adjacent vias, which contributes to a decrease in radial stress beneath the crack. Given that radial stress acts as the primary force initiating delamination, its reduction consequently diminishes the propensity for interfacial delamination in vias spaced at narrower pitch distances. Fig. 31(b) illustrates the impact of the via aspect ratio on the glass wafer, showcasing the effects of reducing the height of the vias (H) and consequently the via aspect ratio (AR = H:D), while keeping the via diameter (D) constant. The figure reveals that as the aspect ratio decreases, there is an observable increase in ERR. This phenomenon occurs due to the intensified stress interaction between the top and bottom ends of the via as its height diminishes. Consequently, this enhanced stress interaction creates a greater driving force for crack initiation in vias with lower aspect ratios.

Ahmed et al. used another 2D FEA model to study the cohesive glass cracking in the heating process with varying design parameters as shown in Fig. 32 [5]. The effect of via pitch is plotted in Fig. 33 showing that as pitch distances decrease, stress interaction leads to a larger ERR along the 0° direction, but a smaller ERR along the 45° direction. Additionally, as depicted in Fig. 34, three via designs were evaluated. The findings, presented in Fig. 35, indicate that the annular via exhibits a lower ERR compared to a solid via. Moreover, the ERR is further diminished in the configuration featuring a substrate-cored via. Zhao et al. employed a 3D model to investigate the influence of a buffer layer, utilizing various

Table 3
Parametric study on TGV using FE modeling.

Model type	Thermal loading (°C)	Stress free temperature (°C)	Material property	Metric	Via type	parameter	Influence on glass	Reference
3D	−55 to 125	50	linear	Max principal stress	Conformal plated	Aspect ratio (H/D)	Larger aspect ratio, higher stress	[70]
						Via diameter	Larger diameter, lower stress	[70]
						Via pitch	Bigger pitch, lower stress	[70]
3D	−55 to 125	Glass 162 Copper 108 Polymer 162	Cu nonlinear	Max principal stress	Conformal plated	Via taper angle	Larger angle, higher stress	[67]
						Via diameter	Larger diameter, lower stress	[67]
						Via pitch	Bigger pitch, lower stress	[6,67]
						Glass CTE	Larger CTE, lower stress	[67]
XY 2D	25 to 400	25	liner	ERR	Fully filled	Via diameter	Larger diameter, higher ERR	[5]
						Via pitch (2 crack orientations)	For crack in 45°, bigger pitch, lower ERR For crack in 0°, bigger pitch, higher ERR	[5,62]
					N/A	Via type	Fully filed > conformal plated > w/buffer	[5]
XZ 2D	400 to 25	400	liner	ERR	Fully filled	Via pitch	Bigger pitch, higher ERR	[62,63]
						Aspect ratio (H/D)	Larger aspect ratio, lower ERR	[63]
					N/A	Via type	Fully filed > conformal plated	[63]
XZ 2D	400 to 25	400	Cu nonlinear	ERR	Fully filled	Annealing temperature	Higher temperature, higher ERR	[62]
3D	25 to 400	25	Cu nonlinear	Max principal stress	Fully filled	Heating rate	Higher rate, higher stress	[35]
3D	260 to 25	260	Cu nonlinear	Max principal stress	Fully filled	Glass CTE	Larger CTE, lower stress	[44]
					Conformal plated	Cu thickness	Larger thickness, higher stress	[44]

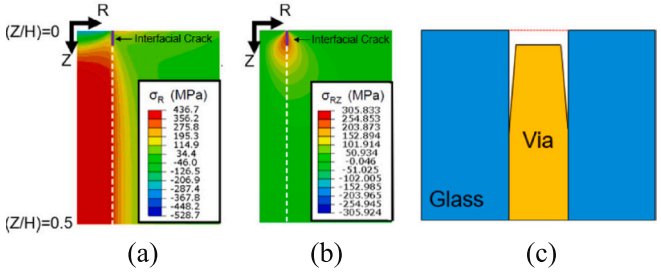

Fig. 30. (a) The distribution of radial stress, (b) the distribution of shear stress, (c) C-cracks on the via/glass interface [63].

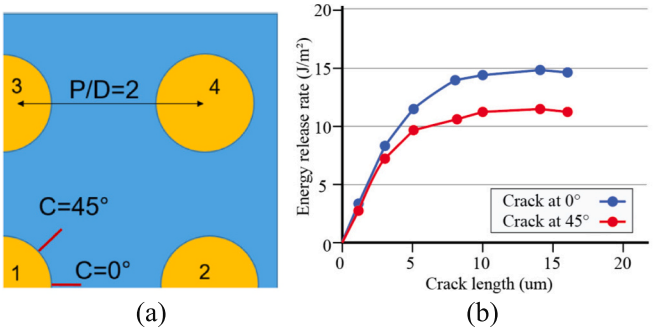

Fig. 32. (a) Two crack configurations with orientations of 0° and 45°, (b) EER with two crack orientations [5].

polymer options, thereby confirming the buffer layer's role in stress mitigation [44].

Considering that fracture analysis is more convenient in 2D models compared to 3D models, Ahmed chose two different 2D models to study TGV behavior during the cooling and heating processes. The XY plane 2D model, shown in Fig. 32, has more restrictions than the XZ plane model, shown in Fig. 30. In real situations, copper protrusion in the Z direction can also produce significant tensile stress, impacting the

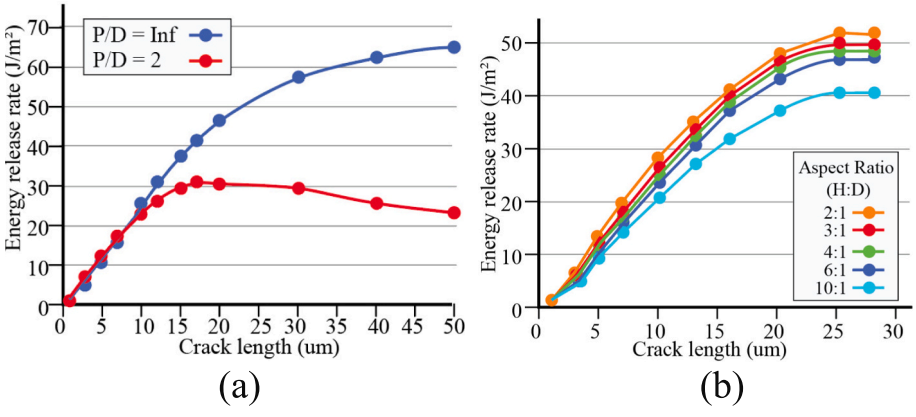

Fig. 31. (a) The effect of the pitch on ERR, (b) the effect of aspect ratio on ERR [63].

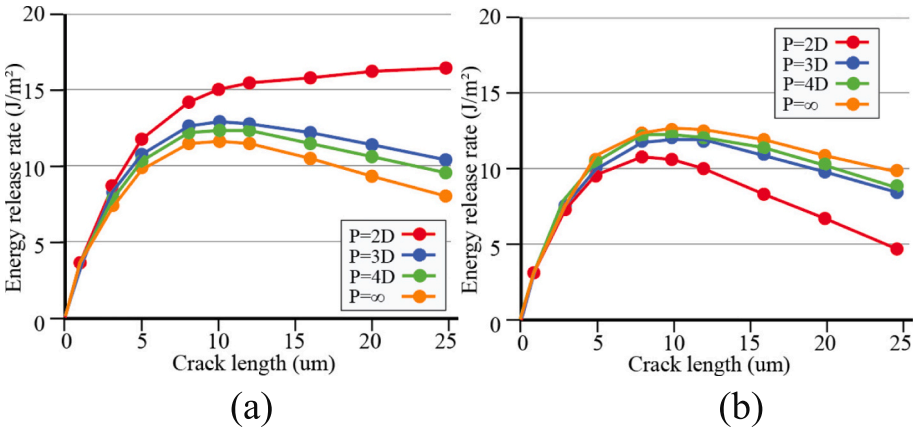

Fig. 33. The effect of pitch distance on ERR (a) crack configurations with orientations of 0°, (b) crack configurations with orientations of 45° [5].

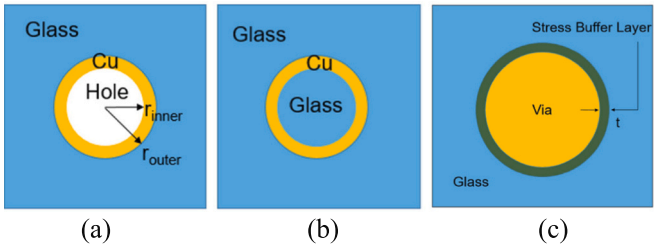

Fig. 34. (a) An annular via, (b) a substrate-cored via, (c) via with buffer layer [5].

integrity of the glass. However, this is not accounted for in the XY plane model. Please note that the reference temperatures used in the heating and cooling models are also different [5,62,63,67]. For Heating, room temperature or copper plating temperature of 50 °C is taken as stress free temperature. For the cooling process, TGVs are assumed to be completely stress relieved after annealing process, so the highest temperature in annealing is used as the reference temperature.

The impact of via diameter on the ERR was examined [5], revealing that an increase in via diameter led to a higher ERR. This rise is attributed to the augmented tangential tensile stress, which is a key factor in mode-I cracking. However, for conformal plated vias, the relationship is reversed, as reported by Demir et al. as shown in Fig. 36 [67,70]. The findings presented in Fig. 37 indicate that smaller conformally plated vias experience higher stress levels. Although the metrics used in the two studies are different, one utilizing maximum principal stress and the other using ERR, the opposing observations are due to the different types of TGVs studied. One study focuses on fully filled vias, while the other examines conformal plated vias. With the thickness of the plated copper remaining constant, an increase in diameter leads to a lower copper percentage per square unit cell, thereby diminishing the effects of CTE mismatch.

The relationship between aspect ratio and the stress on glass in Fig. 37 is opposite to the observation in Fig. 31(b). This discrepancy may be due to the differences in thermal loading conditions, via types, and finite element (FE) modeling methods used in the two studies. As a result, it is difficult to determine if this conflict makes sense.

To date, most FEA modeling efforts aiming at studying TGV lack a direct correlation with experimental outcomes. Only the model developed by Pan was directly validated with displacement measurements obtained by DIC [35,68]. Although a 2D model offers efficiency, a 3D model is more advisable for accounting for the concentrated stress caused by deformation in both the XY plane and the Z direction, as demonstrated in Fig. 36. The boundary condition of the TGV as a unit cell is critical [71]. The author recommends using a quarter model that includes the neighboring TGVs to account for the pitch effect. It is

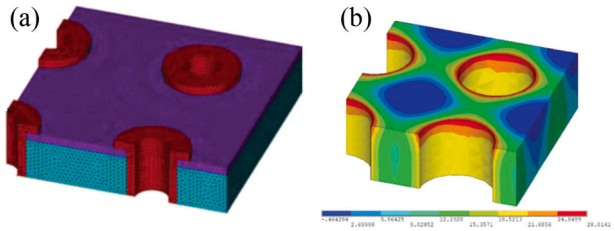

Fig. 36. (a) 3D model mesh, (b) max principal stress contour [67,70].

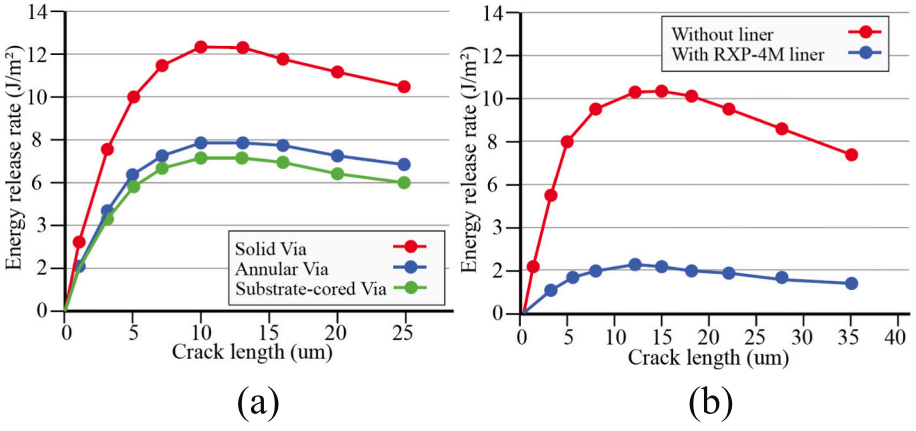

Fig. 35. (a) Comparison of ERRs for the three via designs, (b) the effect of the stress buffer layer on the EER [5].

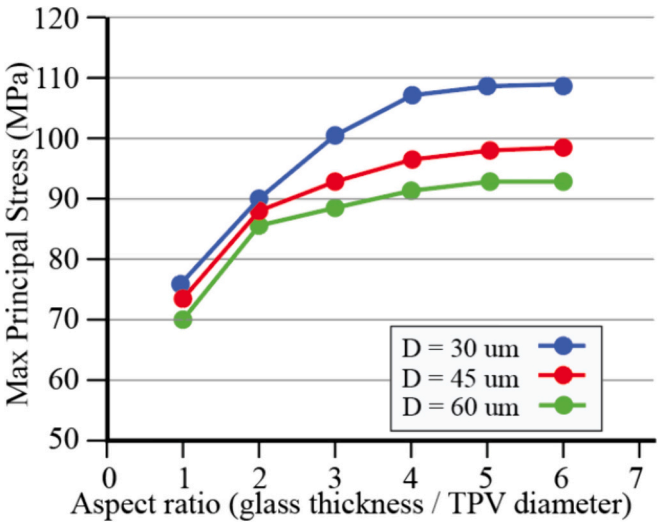

Fig. 37. First principal stress with 3 via diameters [67,70].

advised that all stress and strain data be extracted solely from the center unit.

Both maximum principal stress and ERR are effective metrics for assessing glass fracture. However, fracture modeling has more constraints: (1) it is more effective in 2D modeling rather than 3D modeling, and (2) it depends on crack orientation, meaning one model can only address one type of crack. As shown in Fig. 38, the author studied the influence of TGV pitch during the heating process using XZ-plane 2D models and 3D models, differing from the methods used in two other studies [5,62]. The results of these methods contrast with those using ERR in XY-plane 2D models as shown in Fig. 39. Considering the orientation and size of defects in the glass are unpredictable, using maximum principal stress in a 3D model may be more practical for addressing these problems effectively. Additionally, the selection of material properties for copper should be carefully considered based on thermal loading. The decision to use a creep model in stage 1 or stage 2

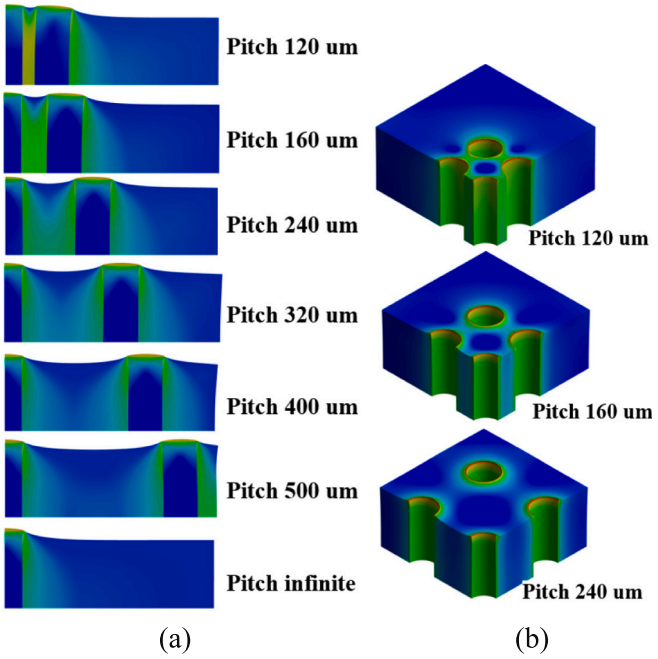

Fig. 38. (a) XZ-plane 2D model, (b) 3D model.

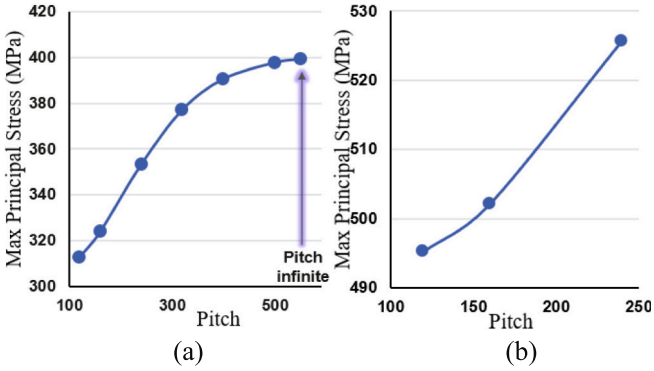

Fig. 39. The influence of pitch on stress (a) 2D model results, (b) 3D model results.

depends on factors such as heating rate, peak temperature, and dwell time.

4. Conclusion

This comprehensive review has illuminated the significant potential and existing challenges associated with the use of glass substrates and TGV in advanced electronic packaging. Glass substrates, with their tunable properties and compatibility with silicon, present a promising alternative to traditional organic materials, offering enhanced performance in terms of dimensional stability, via density, and thermal management. Despite these advantages, our investigation into the thermo-mechanical reliability of these materials has revealed critical hurdles, particularly concerning stress management and the propensity for crack formation under various conditions. Through a detailed examination of fabrication processes, Finite Element Analysis (FEA) models, and experimental studies, we have gained insights into the factors that influence the reliability of glass substrates and TGVs, such as via density, aspect ratios, and the critical role of design parameters like RDL thickness and edge pullback. Furthermore, the introduction of buffer layers and optimized plating processes have emerged as effective strategies for mitigating stress and preventing crack propagation. As the electronic packaging industry continues to evolve, the findings of this review highlight the necessity for ongoing research and development to address the identified challenges. Future work should focus on optimizing fabrication and design techniques to enhance the mechanical and thermal reliability of glass substrates and TGVs. Additionally, the development of standardized testing protocols and the accumulation of long-term reliability data will be crucial for the broader adoption of these materials in next-generation electronic devices. In conclusion, while glass substrates and TGVs hold great promise for revolutionizing electronic packaging, achieving their full potential requires a concerted effort to understand and overcome the thermo-mechanical challenges they present. With continued innovation and collaboration across academia and industry, glass substrates can play a pivotal role in enabling the compact, high-performance electronic devices of the future.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

References

[1] S.R. McCann, V. Sundaram, R.R. Tummala, S.K. Sitaraman, Flip-chip on glass (FCOG) package for low warpage, in: Proceedings - Electronic Components and Technology Conference, 2014, pp. 2189–2193, https://doi.org/10.1109/ECTC.2014.6897606.

[2] M. Shih, K. Chen, T. Lee, D. Tarng, C.P. Hung, FE simulation model for warpage evaluation of glass interposer substrate packages, IEEE Trans. Compon. Packag. Manuf. Technol. 11 (2021) 690–696, https://doi.org/10.1109/TCPMT.2021.3065647.

[3] V. Sukumaran, G. Kumar, K. Ramachandran, Y. Suzuki, K. Demir, Y. Sato, T. Seki, V. Sundaram, R.R. Tummala, Design, fabrication, and characterization of ultrathin 3-D glass interposers with through-package-vias at same pitch as tSVs in silicon, IEEE Trans. Compon. Packag. Manuf. Technol. 4 (2014) 786–795, https://doi.org/10.1109/TCPMT.2014.2303427.

[4] K. Pan, Y. Lai, J. Xu, P. Yin, J. Ha, C. Cai, J. Yang, S. Park, Parametric Study of the Geometry Design of Through-silicon via in Silicon Interposer, InterSociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, ITHERM 2022-May, 2022, https://doi.org/10.1109/iTherm54085.2022.9899623.

[5] O. Ahmed, C. Okoro, S. Pollard, T. Jiang, The effect of materials and design on the reliability of through-glass vias for 2.5 D integrated circuits: a numerical study, Multidiscip. Model. Mater. Struct. 17 (2021) 451–464, https://doi.org/10.1108/MMMS-05-2020-0125.

[6] S. Viswanathan, T. Ogawa, K. Demir, T.B. Huang, P.M. Raj, F. Liu, V. Sundaram, R. Tummala, High frequency electrical performance and thermo-mechanical reliability of fine-pitch, copper-metallized through-package-vias (TPVs) in ultra-thin glass interposers, in: Proceedings - Electronic Components and Technology Conference, 2017, pp. 1510–1516, https://doi.org/10.1109/ECTC.2017.292.

[7] A.O. Watanabe, B.K. Tehrani, T. Ogawa, P.M. Raj, M.M. Tentzeris, R.R. Tummala, Ultralow-loss substrate-integrated waveguides in glass-based substrates for millimeter-wave applications, IEEE Trans. Compon. Packag. Manuf. Technol. 10 (2020) 531–533, https://doi.org/10.1109/TCPMT.2020.2968305.

[8] V. Sukumaran, T. Bandyopadhyay, V. Sundaram, T. Rao, Low-cost thin glass interposers as a superior alternative to silicon and organic interposers for packaging of 3-D ICs, IEEE Trans. Compon. Packag. Manuf. Technol. 2 (2012) 1426–1433, https://doi.org/10.1109/TCPMT.2012.2204392.

[9] R. Tummala, B. Deprospo, S. Dwarakanath, S. Ravichandran, P. Nimbalkar, N. Nedumthakady, M. Swaminathan, Glass panel packaging, as the most leading-edge packaging: technologies and applications, in: 2020 Pan Pacific Microelectronics Symposium 2020, Pan Pacific, 2020, pp. 1–5, https://doi.org/10.23919/PanPacific48324.2020.9059521.

[10] V. Sukumaran, T. Bandyopadhyay, Q. Chen, N. Kumbhat, F. Liu, R. Pucha, Y. Sato, M. Watanabe, K. Kitaoka, M. Ono, Y. Suzuki, C. Karoui, C. Nopper, M. Swaminathan, V. Sundaram, R. Tummala, Design, fabrication and characterization of low-cost glass interposers with fine-pitch through-package-vias, in: Proceedings - Electronic Components and Technology Conference, 2011, pp. 583–588, https://doi.org/10.1109/ECTC.2011.5898571.

[11] L. Liu, D. Nam, B. Guo, J. Ewanchuk, R. Burgos, G.Q. Lu, Glass for encapsulating high-temperature power modules, IEEE J. Emerg. Sel. Top. Power Electron. 9 (2021) 3725–3734, https://doi.org/10.1109/JESTPE.2020.3004021.

[12] Phil Garrou, Intel Glass Core Substrate Update, Packaging IFTLE. https://www.3dincites.com/2024/03/iftle-587-intel-glass-core-substrate-update/, 2024. (Accessed 16 June 2024).

[13] X. Li, X. Jia, J.W. Kim, K.S. Moon, M.B. Jordan, M. Swaminathan, Die-embedded glass interposer with minimum warpage for 5G/6G applications, in: Proceedings - Electronic Components and Technology Conference 2023-May, 2023, pp. 2247–2254, https://doi.org/10.1109/ECTC51909.2023.00389.

[14] V. Sukumaran, Q. Chen, F. Liu, N. Kumbhat, T. Bandyopadhyay, H. Chan, S. Min, C. Nopper, V. Sundaram, R. Tummala, Through-package-via formation and metallization of glass interposers, in: Proceedings - Electronic Components and Technology Conference, 2010, pp. 557–563, https://doi.org/10.1109/ECTC.2010.5490913.

[15] G. Kumar, T. Bandyopadhyay, V. Sukumaran, V. Sundaram, S.K. Lim, R. Tummala, Ultra-high I/O density glass/silicon interposers for high bandwidth smart mobile applications, in: Proceedings - Electronic Components and Technology Conference, 2011, pp. 217–223, https://doi.org/10.1109/ECTC.2011.5898516.

[16] G. Lee, LG Innotek may start development of glass substrates for chip packaging, THE ELEC, Korea Electronics Industry Media, 2024. https://www.thelec.net/news/articleView.html?idxno=4732.

[17] R. Santos, J.P. Delrue, N. Ambrosius, R. Ostholt, S. Schmidt, Processing glass substrate for advanced packaging using laser induced deep etching, in: Proceedings - Electronic Components and Technology Conference 2020-June, 2020, pp. 1922–1927, https://doi.org/10.1109/ECTC32862.2020.00300.

[18] S. McCann, S. Kuramochi, H. Yun, V. Sundaram, M.R. Pulugurtha, R.R. Tummala, S.K. Sitaraman, Board-level reliability of 3D through glass via filters during thermal cycling, in: Proceedings - Electronic Components and Technology Conference 2016-Augus, 2016, pp. 1575–1582, https://doi.org/10.1109/ECTC.2016.362.

[19] C. Kim, D.E. Senior, A. Shorey, H.J. Kim, W. Thomas, Y.K. Yoon, Through-glass interposer integrated high quality RF components, in: Proceedings - Electronic Components and Technology Conference, 2014, pp. 1103–1109, https://doi.org/10.1109/ECTC.2014.6897427.

[20] T. Shi, B. Chou, T.C. Huang, T. Ogawa, Y. Sato, H. Matsuura, S. Kawamoto, V. Sundaram, K. Panayappan, V. Smet, R. Tummala, Design, demonstration and characterization of ultra-thin low-warpage glass BGA packages for smart mobile application processor, in: Proceedings - Electronic Components and Technology Conference 2016-Augus, 2016, pp. 1465–1470, https://doi.org/10.1109/ECTC.2016.372.

[21] B.M.D. Sawyer, Y. Suzuki, R. Furuya, C. Nair, T.C. Huang, V. Smet, K. Panayappan, V. Sundaram, R. Tummala, Design and demonstration of a 2.5-D glass interposer BGA package for high bandwidth and low cost, IEEE Trans. Compon. Packag. Manuf. Technol. 7 (2017) 552–562, https://doi.org/10.1109/TCPMT.2017.2659700.

[22] J. Kim, I. Hwang, Y. Kim, J. Cho, V. Sundaram, R. Tummala, J. Kim, Precise RLGC modeling and analysis of through glass via (TGV) for 2.5D/3D IC, in: Proceedings - Electronic Components and Technology Conference 2015-July, 2015, pp. 254–259, https://doi.org/10.1109/ECTC.2015.7159601.

[23] S. Ravichandran, M. Kathaperumal, M. Swaminathan, R. Tummala, Large-body-sized glass-based active interposer for high-performance computing, in: Proceedings - Electronic Components and Technology Conference 2020-June, 2020, pp. 879–884, https://doi.org/10.1109/ECTC32862.2020.00144.

[24] S. Ravichandran, V. Smet, M. Swaminathan, R. Tummala, Demonstration of glass-based 3D package architectures with embedded dies for high performance computing, in: Proceedings - Electronic Components and Technology Conference 2022-May, 2022, pp. 1114–1120, https://doi.org/10.1109/ECTC51906.2022.00180.

[25] R. Wong, S. Ravichandran, H. Lee, V. Smet, Thermal management of glass panel embedded packages: package architecture vs. power density, in: Proceedings - Electronic Components and Technology Conference 2020-June, 2020, pp. 2105–2106, https://doi.org/10.1109/ECTC32862.2020.00326.

[26] S. Ravichandran, S. Yamada, F. Liu, V. Smet, M. Kathaperumal, R. Tummala, Low-cost non-TSV based 3D packaging using glass panel embedding (GPE) for power-efficient, high-bandwidth heterogeneous integration, in: Proceedings - Electronic Components and Technology Conference 2019-May, 2019, pp. 1796–1802, https://doi.org/10.1109/ECTC.2019.00277.

[27] A.O. Watanabe, M. Ali, R. Zhang, S. Ravichandran, T. Kakutani, P.M. Raj, R. R. Tummala, M. Swaminathan, Glass-based IC-embedded antenna-integrated packages for 28-GHz high-speed data communications, in: Proceedings - Electronic Components and Technology Conference 2020-June, 2020, pp. 89–94, https://doi.org/10.1109/ECTC32862.2020.00027.

[28] S. Erdogan, S. Ravichandran, X. Jia, M. Swaminathan, Characterization of chip-to-package interconnects for glass panel embedding (GPE) for sub-THz wireless communications, in: Proceedings - Electronic Components and Technology Conference 2021-June, 2021, pp. 2328–2333, https://doi.org/10.1109/ECTC32696.2021.00364.

[29] J.W. Kim, X. Li, X. Jia, K.S. Moon, M. Swaminathan, Bottom side cooling for glass interposer with chip embedding using double-sided release process for 6G wireless applications, in: Proceedings - Electronic Components and Technology Conference 2023-May, 2023, pp. 1609–1613, https://doi.org/10.1109/ECTC51909.2023.00273.

[30] X. Jia, X. Li, K.S. Moon, J.W. Kim, K.Q. Huang, M.B. Jordan, M. Swaminathan, Antenna-integrated, die-embedded glass package for 6G wireless applications, in: Proceedings - Electronic Components and Technology Conference 2022-May, 2022, pp. 377–383, https://doi.org/10.1109/ECTC51906.2022.00069.

[31] S. Ravichandran, S. Yamada, T. Ogawa, T. Shi, F. Liu, V. Smet, V. Sundaram, R. Tummala, Design and demonstration of glass panel embedding for 3D system packages for heterogeneous integration applications, J. Microelectron. Electron. Packag. 16 (2019) 124–135, https://doi.org/10.4071/imaps.930748.

[32] M. Kettelgerdes, P. Mezmer, M.J. Haeussler, G. Böttger, M. Tavakolibasti, A. Pandey, H. Erdogan, G. Elger, R. Schacht, B. Wunderle, Realization, multi-field coupled simulation and characterization of a thermo-mechanically robust LiDAR front end on a copper coated glass substrate, in: Proceedings - Electronic Components and Technology Conference 2023-May, 2023, pp. 753–760, https://doi.org/10.1109/ECTC51909.2023.00131.

[33] H. Schröder, L. Brusberg, R. Erxleben, I. Ndip, M. Töpper, N.F. Nissen, H. Reichl, glassPack – a 3D glass based interposer concept for SiP with integrated optical interconnects, in: 2010 Proceedings 60th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, USA 2010, 2010, pp. 1647–1652, https://doi.org/10.1109/ECTC.2010.5490760 (accessed June 8, 2024).

[34] H.Y. Hwang, P. Morrissey, J.S. Lee, P. O'Brien, J. Henriksson, M.C. Wu, T.J. Seok, 128 × 128 silicon photonic MEMS switch package using glass interposer and pitch reducing fibre array, in: 2017 IEEE 19th Electronics Packaging Technology Conference, EPTC 2017 2018-Febru, 2017, pp. 1–4, https://doi.org/10.1109/EPTC.2017.8277436.

[35] K. Pan, J. Xu, Y. Lai, S. Park, C. Okoro, D. Joshi, S. Pollard, In-situ temperature-dependent characterization of copper through glass via (TGV), Microelectron. Reliab. 129 (2022) 114487, https://doi.org/10.1016/j.microrel.2022.114487.

[36] H. Gregory, Glass Substrates Gain Foothold in Advanced Packages, Semiconductor Engineering. https://semiengineering.com/glass-substrates-gain-foothold-in-advanced-packages/, 2024.

[37] S. McCann, V. Smet, V. Sundaram, R.R. Tummala, S.K. Sitaraman, Experimental and theoretical assessment of thin glass substrate for low warpage, IEEE Trans. Compon. Packag. Manuf. Technol. 7 (2017) 178–185, https://doi.org/10.1109/TCPMT.2016.2641164.

[38] H.J. Choi, J.S. Choi, B.J. Park, J.H. Eom, S.Y. Heo, M.W. Jung, K.S. An, S.G. Yoon, Enhanced transparency, mechanical durability, and antibacterial activity of zinc nanoparticles on glass substrate, Sci. Rep. 4 (2014) 2–10, https://doi.org/10.1038/srep06271.

[39] Y.J. Lin, C.C. Hsieh, C.H. Yu, C.H. Tung, D.C.H. Yu, Study of the thermo-mechanical behavior of glass interposer for flip chip packaging applications, in: Proceedings - Electronic Components and Technology Conference, 2011, pp. 634–638, https://doi.org/10.1109/ECTC.2011.5898579.

[40] S. McCann, Design for Mechanical Reliability of Redistribution Layers for Ultra-Thin 2.5D Glass Packages, Georgia Institute of Technology, 2017.
[41] S.R. McCann, Y. Sato, V. Sundaram, R.R. Tummala, S.K. Sitaraman, Study of cracking of thin glass interposers intended for microelectronic packaging substrates, in: Proceedings - Electronic Components and Technology Conference 2015-July, 2015, pp. 1938–1944, https://doi.org/10.1109/ECTC.2015.7159866.
[42] C. Okoro, P. Maurey, S. Pollard, Time and temperature dependence of copper protrusion in metallized through-glass vias (TGVs) fabricated in fused silica substrate, IEEE Trans. Device Mater. Reliab. 21 (2021) 129–136, https://doi.org/10.1109/TDMR.2021.3059227.
[43] K. Pan, C. Okoro, Y. Lai, D. Joshi, S. Park, S. Pollard, A comparative study of the thermomechanical reliability of fully-filled and conformal through-glass via, in: Proceedings - Electronic Components and Technology Conference 2022-May, 2022, pp. 1211–1217, https://doi.org/10.1109/ECTC51906.2022.00194.
[44] J. Zhao, Z. Chen, F. Qin, D. Yu, Thermo-mechanical reliability study of through glass vias in 3D interconnection, Micromachines (Basel) 13 (2022), https://doi.org/10.3390/mi13101799.
[45] How Yuan Hwang, Padraic Morrissey, Jun Su Lee, Peter O'Brien, Johannes Henriksson, Ming C. Wu, Tae Joon Seok, 128 × 128 silicon photonic MEMS switch package using glass interposer and pitch reducing fibre array, in: 2017 IEEE 19th Electronics Packaging Technology Conference (EPTC), Singapore, 2017, pp. 1–4, https://doi.org/10.1109/EPTC.2017.8277436 (accessed June 7, 2024).
[46] T. Wei, Q. Wang, J. Cai, L. Chen, J. Huang, L. Wang, L. Zhang, C. Li, Performance and reliability study of TGV interposer in 3D integration, in: Proceedings of the 16th Electronics Packaging Technology Conference, EPTC 2014, 2014, pp. 601–605, https://doi.org/10.1109/EPTC.2014.7028398.
[47] M. Töpper, I. Ndip, R. Erxleben, L. Brusberg, N. Nissen, H. Schröder, H. Yamamoto, G. Todt, H. Reichl, 3-D thin film interposer based on TGV (Through Glass Vias): an alternative to Si-interposer, in: Proceedings - Electronic Components and Technology Conference, 2010, pp. 66–73, https://doi.org/10.1109/ECTC.2010.5490887.
[48] S. Takahashi, K. Horiuchi, K. Tatsukoshi, M. Ono, N. Imajo, T. Mobely, Development of Through Glass Via (TGV) formation technology using electrical discharging for 2.5/3D integrated packaging, in: Proceedings - Electronic Components and Technology Conference, 2013, pp. 348–352, https://doi.org/10.1109/ECTC.2013.6575594.
[49] C. Okoro, S. Jayaraman, S. Pollard, Understanding and eliminating thermo-mechanically induced radial cracks in fully metallized through-glass via (TGV) substrates, Microelectron. Reliab. 120 (2021) 114092, https://doi.org/10.1016/j.microrel.2021.114092.
[50] A.B. Shorey, S.F. Nelson, D. Levy, P. Ballentine, Glass solutions for wafer level packaging, in: 2019 International Wafer Level Packaging Conference, IWLPC 2019, 2019, pp. 1–6, https://doi.org/10.23919/IWLPC.2019.8914119.
[51] C. Blancher, M. Kathaperumal, F. Liu, M. Swaminathan, Demonstration of eight metal layer redistribution on glass substrate with fine features and microvia, in: Proceedings - Electronic Components and Technology Conference 2023-May, 2023, pp. 1744–1748, https://doi.org/10.1109/ECTC51909.2023.00298.
[52] S. Kuramochi, H. Kudo, M. Akazawa, H. Mawatari, M. Tanaka, Y. Fukuoka, Glass interposer technology advances for high density packaging, in: 2016 IEEE CPMT Symposium Japan, ICSJ 2016, 2016, pp. 213–216, https://doi.org/10.1109/ICSJ.2016.7801263.
[53] V. Sukumaran, T. Bandyopadhyay, V. Sundaram, T. Rao, Low-cost thin glass interposers as a superior alternative to silicon and organic interposers for packaging of 3-D ICs, IEEE Trans. Compon. Packag. Manuf. Technol. 2 (2012) 1426–1433, https://doi.org/10.1109/TCPMT.2012.2204392.
[54] P. Brown, Glass-based semiconductor fab breaks ground, Electronics360 (n.d.). https://electronics360.globalspec.com/article/18846/glass-based-semiconductor-fab-breaks-ground.
[55] S. McCann, Y. Sato, V. Sundaram, R.R. Tummala, S.K. Sitaraman, Prevention of cracking from RDL stress and dicing defects in glass substrates, IEEE Trans. Device Mater. Reliab. 16 (2016) 43–49, https://doi.org/10.1109/TDMR.2015.2507978.
[56] S. McCann, B. Singh, V. Smet, V. Sundaram, R.R. Tummala, S.K. Sitaraman, Process innovations to prevent glass substrate fracture from RDL stress and singulation defects, IEEE Trans. Device Mater. Reliab. 16 (2016) 622–630, https://doi.org/10.1109/TDMR.2016.2614246.
[57] S. McCann, Y. Sato, T. Ogawa, R.R. Tummala, S.K. Sitaraman, Use of birefringence to determine redistribution layer stresses to create design guidelines to prevent glass cracking, IEEE Trans. Device Mater. Reliab. 17 (2017) 585–592, https://doi.org/10.1109/TDMR.2017.2738625.
[58] Y. Lai, C. Cai, K. Pan, J. Yang, J. Ha, P. Yin, K. Deo, S. Park, THERMOMECHANICAL RELIABILITY of BGA PACKAGES with DIFFERENT UNDERFILL REINFORCEMENT METHODS, in: Proceedings of ASME 2022 International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems, InterPACK 2022, 2022, pp. 1–6, https://doi.org/10.1115/IPACK2022-97349.
[59] M.K. Shih, C. Hsu, Y. Chang, K. Chen, I. Hu, T. Lee, D. Tarng, C.P. Hung, Warpage characterization of glass interposer package development, in: Proceedings - Electronic Components and Technology Conference, 2017, pp. 1392–1397, https://doi.org/10.1109/ECTC.2017.110.
[60] V. Jayaram, O. Gupte, V. Smet, Modeling and design for system-level reliability and warpage mitigation of large 2.5D glass BGA packages, in: Proceedings - Electronic Components and Technology Conference 2022-May, 2022, pp. 1060–1067, https://doi.org/10.1109/ECTC51906.2022.00171.
[61] G.R. Trott, A. Shorey, Glass wafer mechanical properties: a comparison to silicon, in: 2011 6th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT), 2011, pp. 359–362.
[62] X.B. Le, S.H. Choa, A comprehensive numerical analysis for preventing cracks in 2.5D glass interposer, J. Mech. Sci. Technol. (2024), https://doi.org/10.1007/s12206-024-0522-1.
[63] O. Ahmed, G. Jalilvand, S. Pollard, C. Okoro, T. Jiang, The interfacial reliability of through-glass vias for 2.5D integrated circuits, Microelectron. Int. 37 (2020) 181–188, https://doi.org/10.1108/MI-04-2020-0020.
[64] C. Okoro, A.Y. Park, T. Allowatt, S. Pollard, Elimination of thermo-mechanically driven circumferential crack formation in copper through-glass via substrate, IEEE Trans. Device Mater. Reliab. 21 (2021) 354–360, https://doi.org/10.1109/TDMR.2021.3096931.
[65] K.E. Pan, Thermomechanical Reliability and Constitutive Investigation of Copper Through-Glass Via in Glass, Binghamton University, 2022.
[66] K. Demir, K. Ramachandran, Y. Sato, Q. Chen, V. Sukumaran, R. Pucha, V. Sundaram, R. Tummala, Thermomechanical and electrochemical reliability of fine-pitch through-package-copper vias (TPV) in thin glass interposers and packages, in: Proceedings - Electronic Components and Technology Conference, 2013, pp. 353–359, https://doi.org/10.1109/ECTC.2013.6575595.
[67] K. Demir, V. Sukumaran, Y. Sato, A. El Amrani, K. Ramachandran, R. Pucha, P. Markondeya Raj, V. Sundaram, R. Tummala, Reliability of fine-pitch through-vias in glass interposers and packages for high-bandwidth computing and communications, J. Mater. Sci. Mater. Electron. 29 (2018) 12669–12680, https://doi.org/10.1007/s10854-018-9384-6.
[68] K. Pan, J. Yang, Y. Lai, S. Park, C. Okoro, D. Joshi, S. Pollard, High-temperature constitutive behavior of electroplated copper TGV through numerical simulation, IEEE Trans. Compon. Packag. Manuf. Technol. 13 (2023) 1861–1867, https://doi.org/10.1109/TCPMT.2023.3322423.
[69] K. Pan, J. Xu, Y. Lai, S. Park, C. Okoro, D. Joshi, S. Pollard, Investigation of copper and glass interaction in Through Glass Via (TGV) during thermal cycling, in: Proceedings - Electronic Components and Technology Conference 2021-June, 2021, pp. 1660–1666, https://doi.org/10.1109/ECTC32696.2021.00263.
[70] K. Demir, A. Armutlulu, V. Sundaram, P.M. Raj, R.R. Tummala, Reliability of copper through-package vias in bare glass interposers, IEEE Trans. Compon. Packag. Manuf. Technol. 7 (2017) 829–837, https://doi.org/10.1109/TCPMT.2017.2691407.
[71] J. Yang, K. Pan, P. Yin, Y. Lai, S. Park, C. Okoro, D. Joshi, S. Pollard, Adhesion layer influence on thermomechanical reliability of electroplated copper Through-Glass Via (TGV), 2024 IEEE 74th Electronic Components and Technology Conference (ECTC), Denver, CO, US (2024) 1820–1825. doi:https://doi.org/10.1109/ECTC51529.2024.00304.