ASME Journal of Electronic Packaging
Online journal at:
https://asmedigitalcollection.asme.org/electronicpackaging

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A Comprehensive Study on Characterization of Residual Stress of Build-Up Layer and Prediction of Chip Warpage

Better understanding and control of residual stress in the chip build-up layer are becoming more and more important for the assembly process. To estimate the chip warpage and characterize the residual stress, different methods are proposed. However, most of them have high cost or some limitations for the upper build-up material. In this study, an innovative method is proposed to characterize the residual stress and predict the chip warpage behavior of different size chips at different temperatures. The method combines experimental inspection of chip warpage and finite element analysis. By reducing the silicon die thickness, the influence of residual stress in the build-up layer can be amplified. The residual stress can be obtained by inspecting the increased warpage when the silicon dies are reduced to different thicknesses. Correlating the thermal increase warpages of thinner chips can help characterize the effective modulus and coefficient of thermal expansion (CTE) of the build-up layer. This study can help better understand the commonly classified build-up layer information. The results show good agreements between two types of samples under the same upstream process flow. [DOI: 10.1115/1.4063919]

1 Introduction

The flip chip technology has been extensively used to achieve high I/O density for chips to be attached to the substrate in electronic packages [1]. To fabricate the chips on flip chip packages, a multilayered build-up structure, which is known as back end of line, is manufactured on the bulk silicon die, as shown in Fig. 1 [2]. Such sequential build-up process may induce residual stress that is caused collectively by various factors, including thermal mismatch, mechanical deformation, and phase transformation. When the chip is relatively thick, such kind of residual stress may not cause a big influence, yet for thinner chips, stress-caused warpages will be amplified and bring reliability concerns to the package. Therefore, it is important to characterize the residual stress and evaluate the chip deflection during the assembly process.

Many methods have been developed to evaluate the residual stress of the thin film/substrate system like X-ray diffraction, indentation facture, and curvature measurement [3–5]. Additionally, the integration of digital image correlation (DIC) techniques with finite element modeling analysis has been instrumental in quantifying residual stresses. DIC allows for the measurement of strain fields on the surface of electronic components, which can then be used to infer the underlying residual stresses through finite element modeling simulations [6–8]. This hybrid approach has proven valuable in understanding stress redistribution under thermal cycling and mechanical loading conditions. The X-ray diffraction can only be used when the top film is crystalline material [9]. Curvature measurement is commonly used in chip evaluation as it is nondestructive and convenient. According Stoney equation, the stress can be calculated by measuring the curvature of the chip by 3D DIC or Shadow Moiré [10,11]. However, the presence of surface microbumps on chips adds complexity to the situation and certain thick chips with small scale may have warpage that is smaller than the accuracy limit of the measurement tool. Moreover, this method could not obtain the Young's modulus and CTE value of build-up layer as they are usually classified. In this paper, a comprehensive method combining warpage measurement and finite element analysis is proposed. With this method,

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Contributed by the Electronic and Photonic Packaging Division of ASME for publication in the Journal of Electronic Packaging. Manuscript received June 27, 2023; final manuscript received September 22, 2023; published online November 23, 2023. Assoc. Editor: Ming-Yi Tsai.

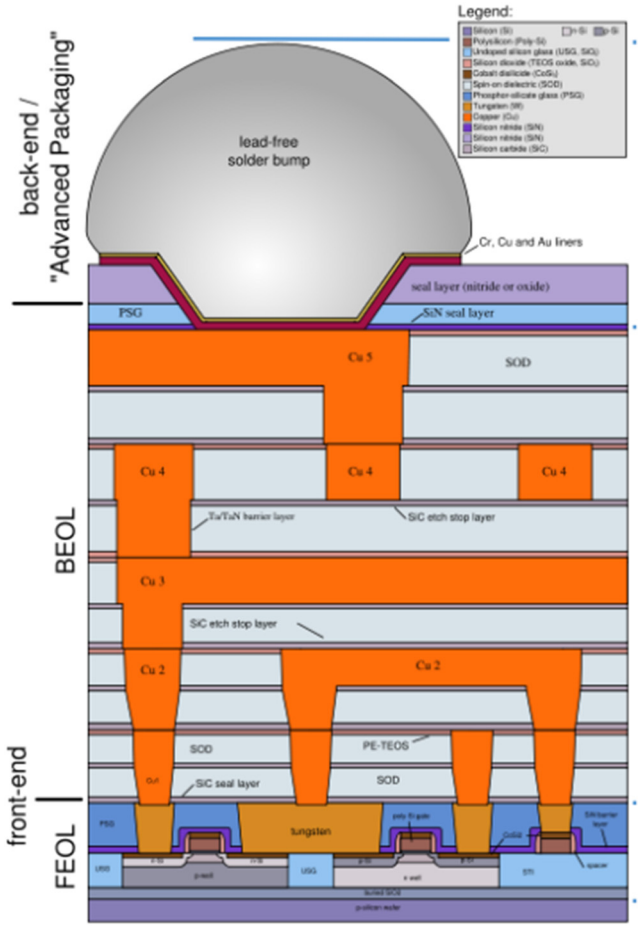

Fig. 1 Schematic of build-up structure

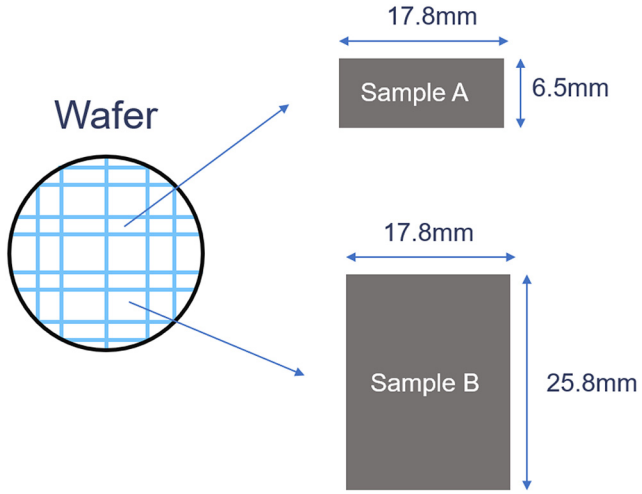

Fig. 2 Two types of samples diced from the same wafer

the residual stress of build-up layer can be evaluated. Besides, the effective Young's modulus and CTE value of the layer can also be fitted for warpage estimation.

In study, manufactured chips with original thickness of 800 μm were grinded to difference thickness targeting 400, 200, and 100 μm to remove the bulk silicon so that the effect of residual stress can be amplified to cause bigger warpage. The majority portion of surface C4 bumps and copper pillars is also grinded to reduce the influence of warpage. With the silicon thickness drop off, the impact of build-up layer stress will increase and the warpage at each thickness is more obvious and can be measured when the die thickness is reduced. After the grinding process, the chip warpage at different elevated temperature can also be obtained. With this data, a finite element model was built to apply fictitious stress on chips, the simulated warpage was tuned to correlate the experimental value and the Young's modulus, and CTE of build-up layer can also be calculated by multiparameter regression. To prove the validity of the fitted simulation results, the stress and material properties were applied into the Stoney equation, both the analytical solution and simulation results showed good agreement with the experimental warpage. With this grinding and characterizing methodology, we are able to not only predict the warpage of the chips in this study at different thickness and temperature, but also more importantly, to evaluate the residual stress and material property of build-up layer when dealing with unknown chips in the future.

2 Experimental Setup

As shown in Fig. 2, two types of samples are obtained from the diced wafer. We classify the two different sizes of chips as type A samples and type B samples. The schematic of chip samples is shown in Fig. 3. The silicon layer has a thickness of 725 μm and the build-up layer thickness is less than 10 μm. On the top of the build-up layer, an array of microbumps is planted. They consist of 75 μm thickness together with the build-up layer.

To minimize the influence of microbumps, the bumps were grinded while maintaining a 30 μm height to prevent overgrinding of the buildup layer considering our manual grinding accuracy capacity. Figure 4 shows the sectional image of build-up layer and remaining bumps after grinding.

Due to the fact that silicon is very brittle and tends to break easily when it gets thinner, the dies were grinded to four stages of thickness. For type A samples, the silicon part was grinded from 725 μm to different thicknesses: 400, 200, and 100 μm. For type B samples, the chips need extra cautious handling because of their larger size. The yield rate for 100 μm thickness type B samples is very low due to the breakage of chips during grinding; thus, type B samples were only grinded to the minimal thickness of 200 μm. Type A samples showed detectable warpages when silicon die is reduced to less than 200 μm while type B samples showed obvious warpage at 400 μm thickness due to larger size. The samples were heated from 25 °C to 250 °C when obvious warpages were detected.

The schematic of different sample thickness stages is shown in Fig. 5. After reaching the thickness target, samples were inspected using the Takaoka confocal inspection tool. It is a nondestructive tool that does not require surface treatment to measure the warpage [12]. The warpage of chips was measured after the silicon part was removed to different extents. Based on the curvature of the chips after grinding, we would be able to characterize the residual stress in the later analysis. The schematic of Takaoka confocal warpage inspection tool is shown in Fig. 6.

The silicon dies were grinded using sandpapers with different grits that the finest was 3000 grits. After grinding, the thicknesses of the chips was measured by calculating the average thickness results inspected by optical microscope. Three samples were prepared for each thickness stage for type A samples to characterize and analyze the residual stress result (12 samples in total). Since type A and type B samples were diced from the same wafer, the residual stress in type B samples should be the same with type A samples as they went through the same process flow. Considering the capability of the grinding facility, after the investigation of type A samples, one chip was prepared for each stage of type B samples to verify the results (4 samples in total). The target silicon thickness and the actual silicon thickness at different stages are shown in Table 1.

3 Results and Discussions

After grinded to different stages of thickness, the warpage of the chip was inspected, the typical warpage contour of the sample is

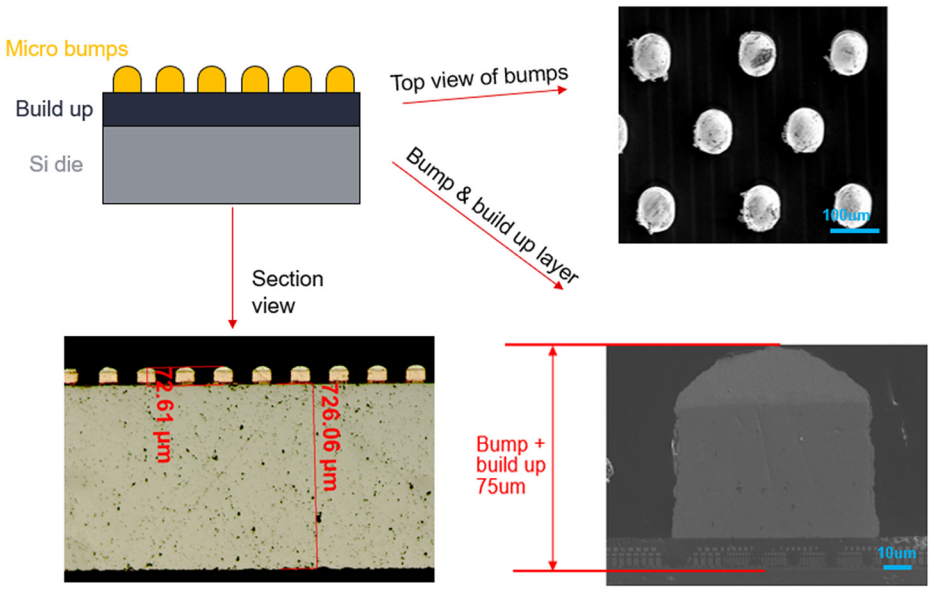

Fig. 3 Schematic and section view of the chip and build-up layer

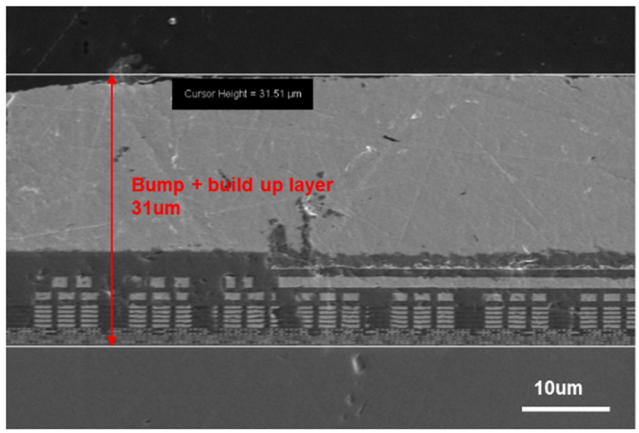

Fig. 4 Section image of the build-up layer and remaining bump

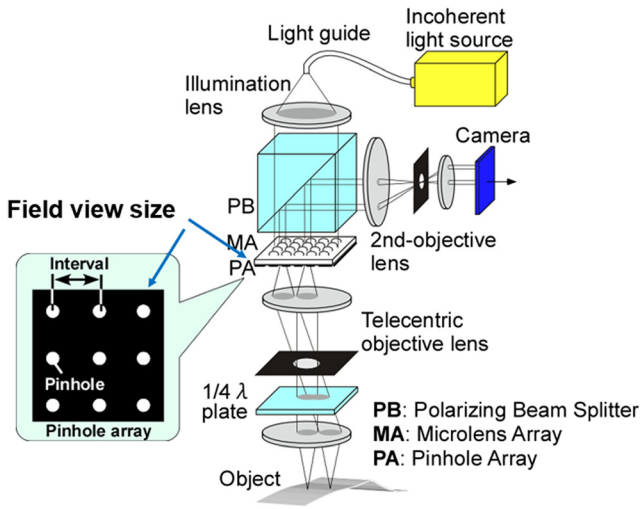

Fig. 6 Schematic of Takaoka warpage inspection tool

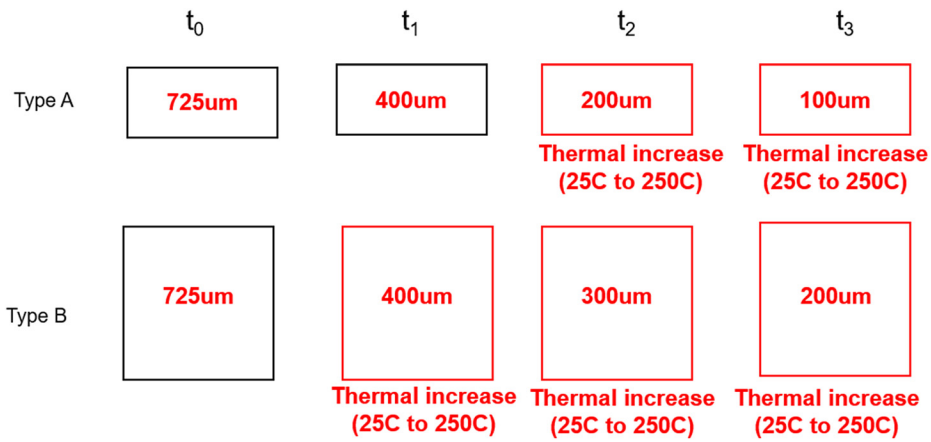

Fig. 5 Different stages of die thickness reduction for type A and B samples

Table 1 Samples with different thicknesses

Sample type	Stage No.	Target thickness (μm)	Actual thickness (μm)		
Type A	t_0	725	725	725	725
	t_1	400	385	385	400
	t_2	200	185	180	200
	t_3	100	70	75	95
Type B	t_0	725	725		
	t_1	400	385		
	t_2	300	275		
	t_3	200	170		

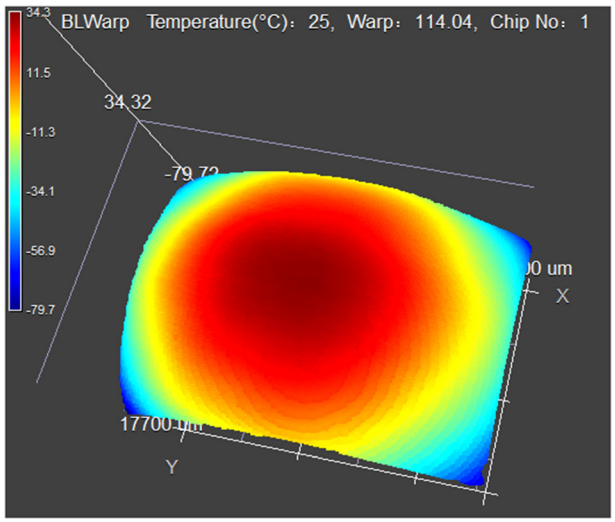

Fig. 7 Type B sample warpage contour at room temperature when grinded to t_3 stage

shown in Fig. 7. The contour is symmetric, and thus warpage pattern can be characterized by the warpage plot along the diagonal line.

3.1 Type A Samples Results. The warpage of type A samples was first investigated. At room temperature, the warpages of the samples from t_0 stage to t_3 stage (725, 385, 185, and 70 μm) are shown in Fig. 8. The confocal measurement equipment capability is within ± 2 μm. It can be seen that at t_0 and t_1 stages, due to the bulk volume of the silicon, the warpage is less than 2 μm and cannot be

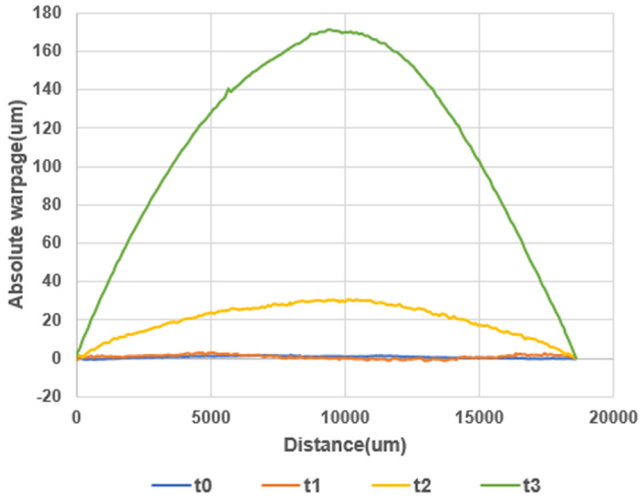

Fig. 8 Type A sample warpage contour at room temperature when grinded from t_0 to t_3 stage

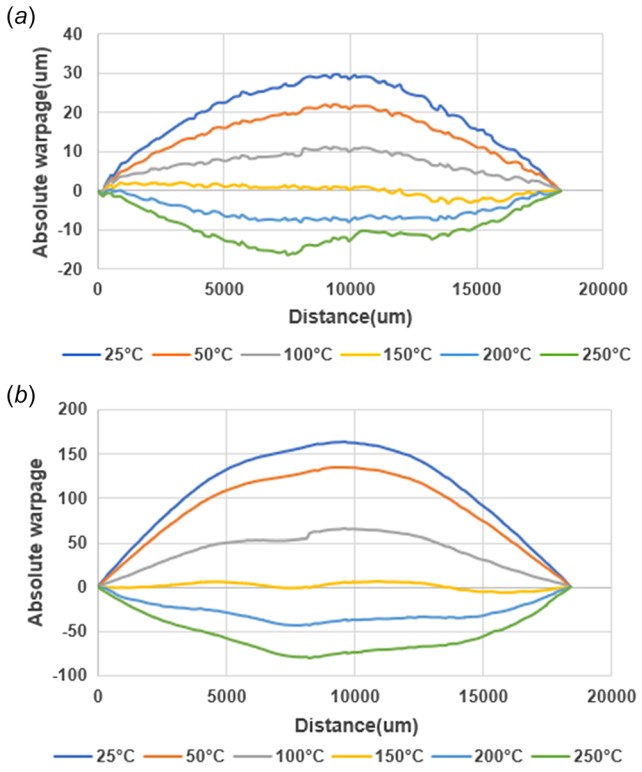

Fig. 9 Warpage change of type A sample when heated, (*a*) sample with 185 μm silicon die thickness and (*b*) sample with 75 μm silicon die thickness

detected by the inspection tool. However, when the die thickness is reduced to less than 200 μm, the impact of the residual stress becomes more obvious. The warpage of the chip increased exponentially when the die thickness is further decreased. From Fig. 8, it can be indicated that the maximum warpage of the chip curvature would have nonlinear increase with respect to the die thickness.

To gain a better understanding of the chip's behavior under thermal stress, samples at t_2 and t_3 stages underwent heating from room temperature 25 °C to 250 °C. Figure 9 shows the warpage changes observed in samples with thicknesses of 185 μm and 75 μm. With silicon surface facing upside, the chips showed concave curvature at room temperature. The negative value indicates convex shape, the positive value indicates concave shape (die side facing up). When the temperature increases, the maximum warpage decreases and reaches close to zero at around 150 °C for both samples. At temperature higher than 150 °C, the sample showed

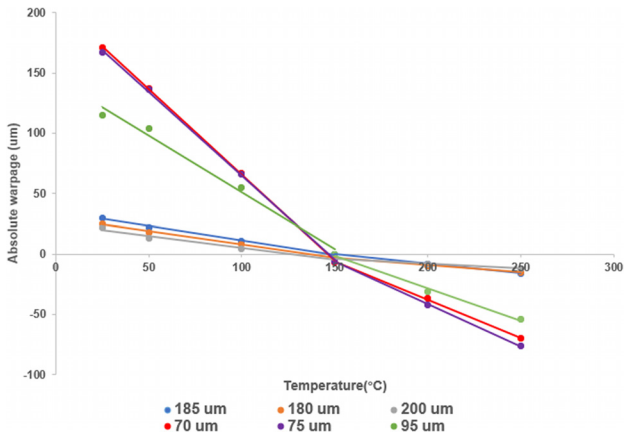

Fig. 10 Warpage change of t_2 and t_3 type A samples when heated

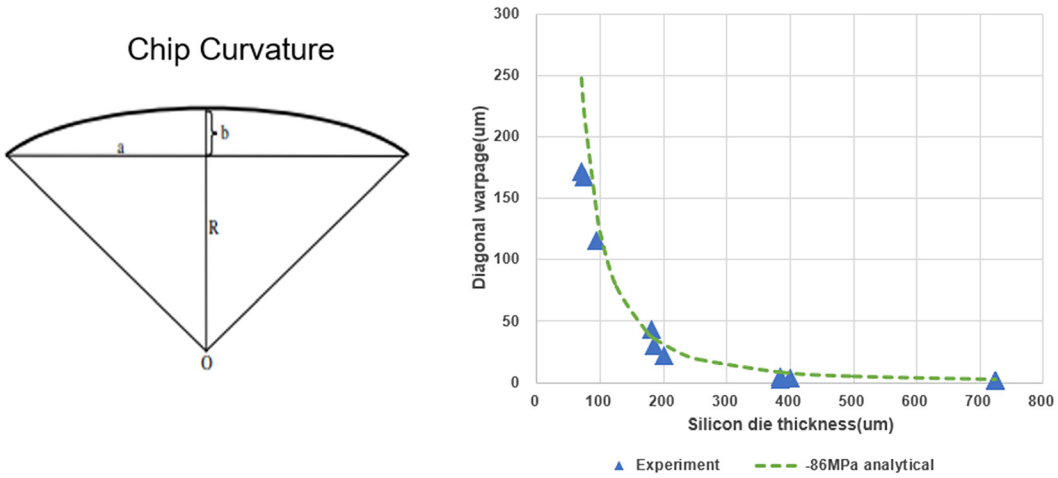

Fig. 11 Schematic and fitting of Stoney equation results

convex curvature and warpage increase with respect to temperature. Based on the previous observation, 150 °C can be considered as a stress-free temperature.

The summary of the six samples under thermal increase process is shown in Fig. 10. The maximum warpages at different temperatures for each sample are listed. The data show a good linear fit before and after 150 °C. According to the analytical analysis of package warpage, the chip warpage is directly related to the Yong's modulus and CTE combination [13]. In this study, the residual stress also contributes to the out-of-plane deformation. Considering that the residual stress is inherently introduced during the process flow and remains a constant, we can lump this factor together with the thermal effect to simplify the analysis. Thus the "effective modulus and CTE" we discuss here may not be the actual physical material properties of the build-up layer, but it may help us characterize the total stress including residual stress and thermal stress and predict the warpage precisely in the future. According to Fig. 10, the effective modulus and CTE may change after 150 °C as the slope of the fitting lines change apparently.

Before the effective modulus and CTE are specified, the residual stress of the build-up layer can be evaluated first based on the room temperature warpage results. According to the Stoney equation, the stress of bilayer system can be identified as follows [14]:

$$\sigma = \frac{E}{6(1-\nu)}\frac{t_s^2}{t_f}\frac{1}{R} \tag{1}$$

$$(R-b)^2 + \left(\frac{a}{2}\right)^2 = R^2 \tag{2}$$

$$R = \frac{b}{2} + \frac{a^2}{8b} \tag{3}$$

where t_s is die thickness and t_f is the build-up layer thickness. The schematic of a, b, and R is shown in Fig. 11. Type A sample has the diagonal length $a = 18{,}950\ \mu$m and b is the maximum warpage. As a result, the relationship between residual stress and warpage can be described as

$$\sigma = \frac{E}{6(1-\nu)}\frac{t_s^2}{t_f}\frac{8b}{4b^2+a^2} \tag{4}$$

Since we already have the warpage results, the residual stress can be correlated to fit the experimental data. The stress results based on the analytical method are tuned as around 86 MPa. The comparison of the analytical curve versus the experimental results is shown in Fig. 11.

Besides that, the warpage at room temperature can also be characterized based on the finite element model. The model only included a silicon block, and the residual stress was applied on the surface nodes by using the INISTATE command. The directional displacement can be fitted compared to the experiment warpage and the residual stress can be characterized by investigating the impacted area near the top surface, as shown in Fig. 12.

Figure 13 demonstrates that by applying prestress to match the experimental warpage, the residual stress on the die aligns with the analytical method. To account for the impact of thermal stress and enable the prediction of chip warpage at elevated temperatures, it becomes necessary to ascertain the effective modulus and CTE for the build-up layer. In this context, we constructed an FEA model that incorporates both the silicon die and the effective build-up layer. Some researchers have performed certain studies to analyze the

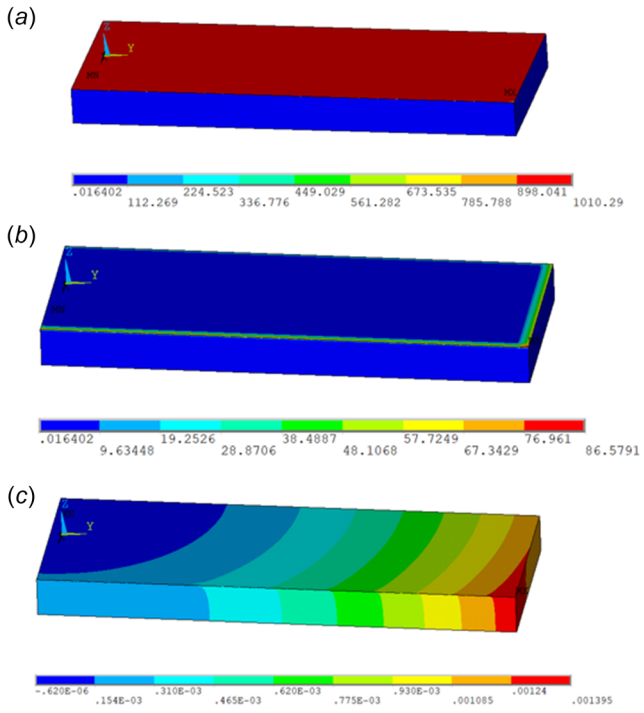

Fig. 12 FEA model results in MPa, (*a*) prestress applied on the surface nodes of the model, (*b*) residual stress influence on the die, and (*c*) directional displacement at room temperature with 725 μm silicon die thickness

individual layer material property of buildup layer, yet due to the structural difference, the effective modulus and CTE values may vary [15]. Usually, the structural information of the build-up layer is classified; thus, it would be meaningful to obtain those values as a knob to characterize the thermal mechanical behavior of different size of chips with different thicknesses. The back end of line layer consists of copper, silicon, silicon oxide, ELK, and low k material. The DOE was performed based on the literature survey to find the reasonable material property range [16]. A DOE of modulus varying from 15 GPa to 50 GPa with increment of 0.1 GPa and CTE varying from 3 ppm/°C to 20 ppm/°C with increment of 0.1 ppm/°C was performed to find the optimum recipe with minimal deviation from the experimental thermal increase warpage results. Poison's ratio would also contribute to the deformation [17] yet in this case, the value is simplified as 0.3 based on the literature results [18]. Because the slope changes after 150 °C, the modulus was fitted separately before 150 °C and after 150 °C while CTE is assumed to be a constant.

After the modulus and CTE are set to 44.6 GPa, CTE 12.6 ppm/°C before 150 °C and 23.3 GPa, CTE 12.6 ppm/° C. The simulation results can be fitted well with the experimental results, as shown in Fig. 14.

The schematic of the FEA model with build-up layer and silicon chip is shown in Fig. 15(*a*). To further validate the modeling, the stress at 25 °C is shown in Fig. 15(*b*), the stress is close to 86 MPa which is consistent with our previous room temperature residual stress study. The overall plot in Fig. 15(*c*) includes both the room temperature and thermal increase data. The warpage of the chip

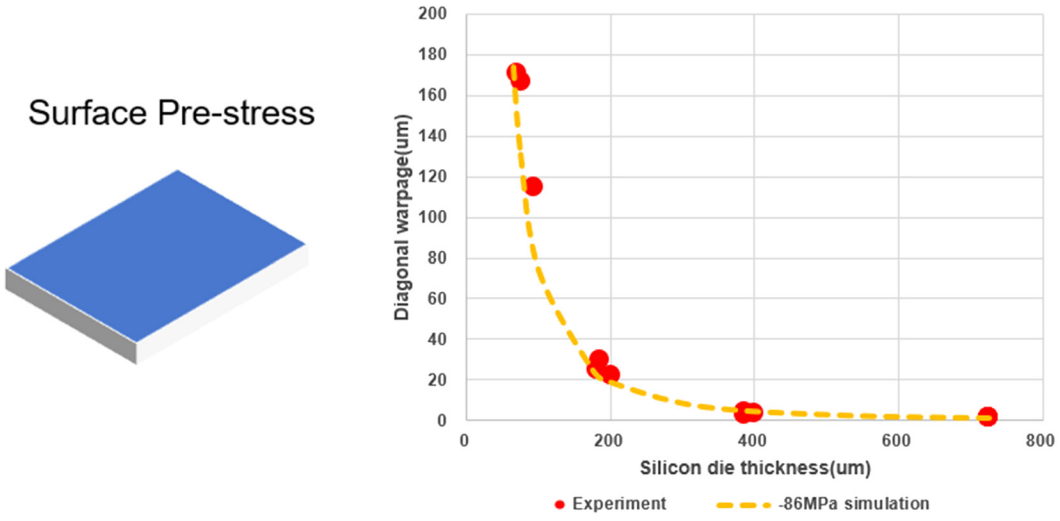

Fig. 13 Schematic and fitting of simulation results

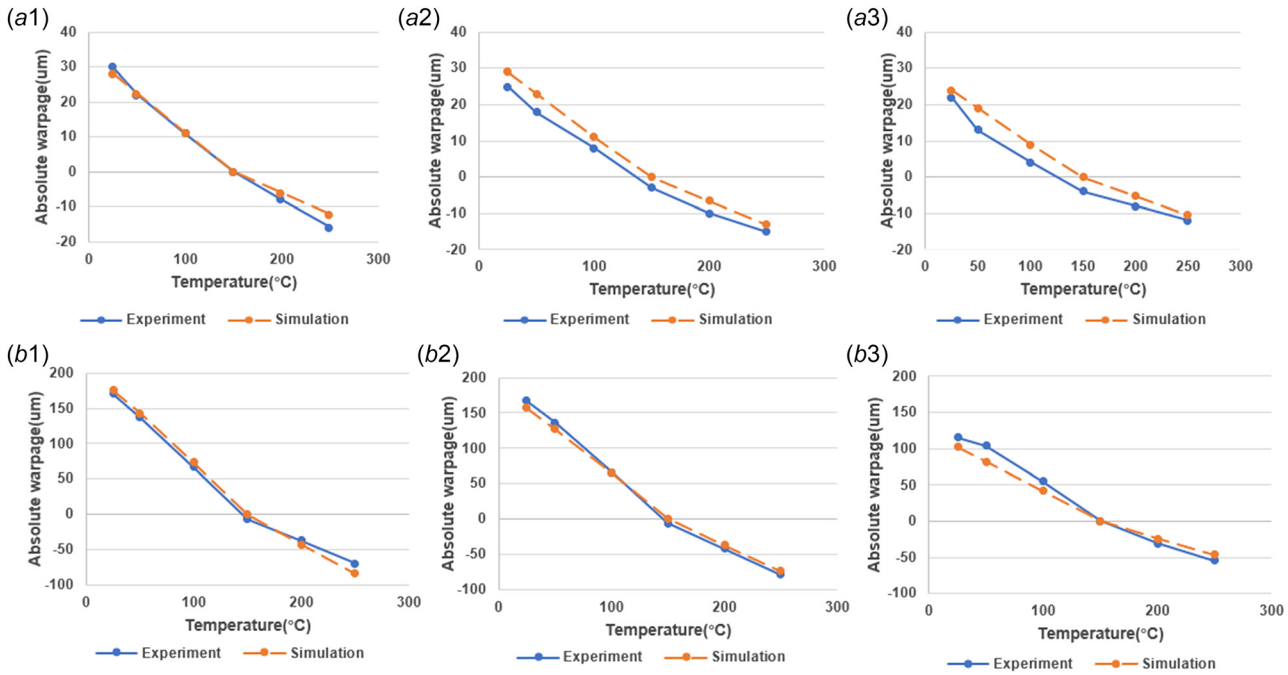

Fig. 14 Warpage comparison between simulation and experiment for t_2 and t_3 type A samples, (a1) 185 μm, (*a*2) 180 μm, (*a*3) 200 μm, (*b*1) 70 μm, (*b*2) 75 μm, and (*b*3) 95 μm

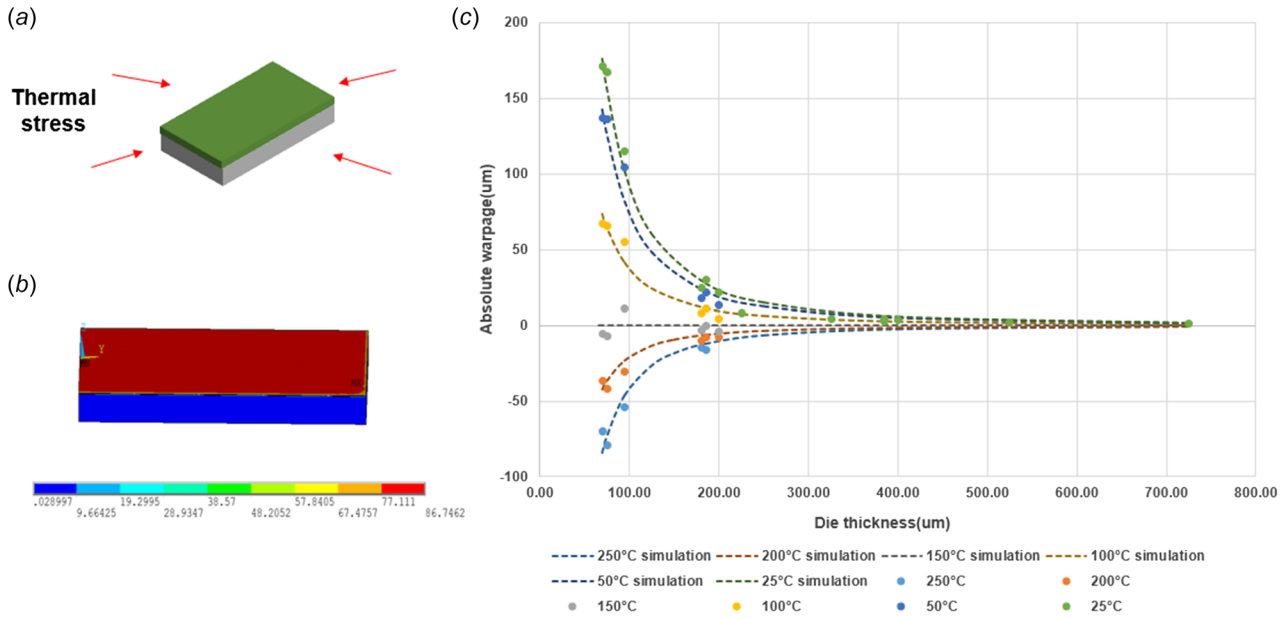

Fig. 15 Type A sample warpage comparison between simulation and experiment, (*a*) model schematic, (*b*) stress at room temperature, and (*c*) overall comparison between model and all type A samples results

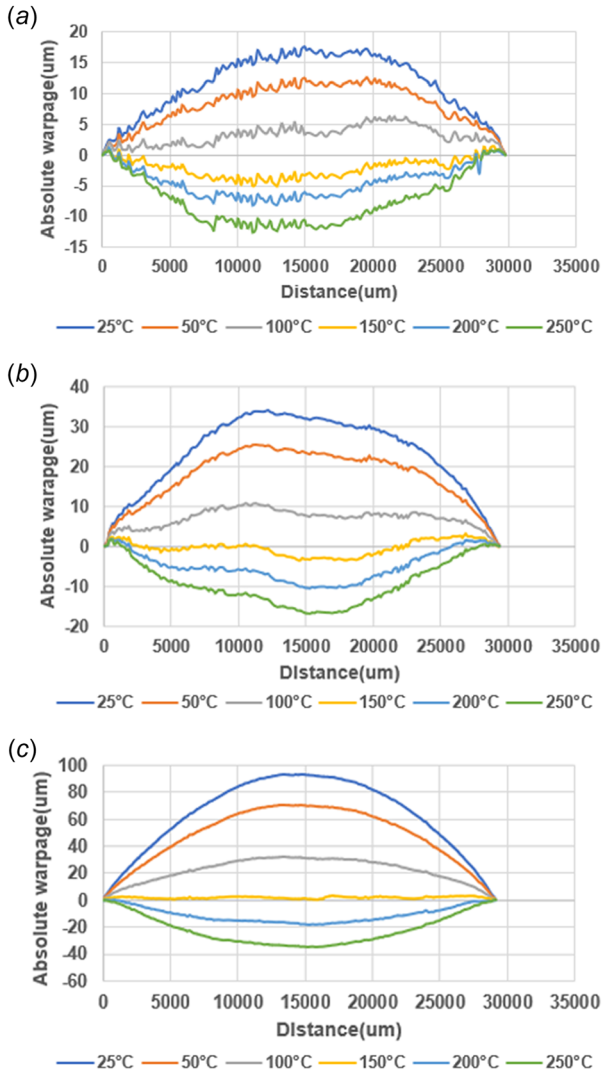

Fig. 16 Warpage change of type B sample when heated, (*a*) sample with 385 μm silicon die thickness, (*b*) sample with 275 μm silicon die thickness, and (*c*) sample with 170 μm silicon die thickness

increases nonlinearly when the die thickness is reduced till less than 100 μm for type A samples.

3.2 Type B Samples Results. To validate the residual stress and effective modulus as well as CTE results, type B samples, chips with larger size than type A samples were inspected. They are supposed to have the same residual stress and material properties as they come from the same wafer.

Four samples with different thicknesses were measured. Figure 16 shows the warpage change when the die thickness was reduced from t_1 stage to t_3 stage. The results show that the warpage is close to zero near 150 °C.

To validate the results that we got from type A samples, the effective modulus and CTE value are applied into the FEA model with changed chip size to calculate the warpage results. The FEA results based on the previous inputs are shown in Fig. 17. The comparison shows good agreement with the experimental results. For type B samples, before 150 °C and after 150 °C the slopes show similar changes.

The stress at room temperature is also evaluated. Figure 18(*a*) shows the same 86 MPa results, the overall data include both room temperature and thermal increase warpage values. As shown in Fig. 18(*b*), the simulation shows consistent output with experimental data after applying inputs calculated from type A samples.

4 Conclusion

In this study, an innovative method is proposed to investigate the residual stress inside the build-up layer caused by the process flow. The effective modulus and CTE of the build-up layer were also characterized to represent and predict the warpage behavior of the chips under different thermal conditions. It can provide an effective way to estimate the curvature of chips with different scales and thicknesses. As a result, we can assess the risk and capability during the assembly process and further approximate the warped bonded dies.

Two different types of samples are studied. We focused on samples with smaller size because they are more handling-friendly. The residual stress can be quantified and the obtained effective modulus and CTE are applied to calculate the warpage of larger size type B samples. The validation results show good agreement with the fitted material property recipe. With these achieved results, we

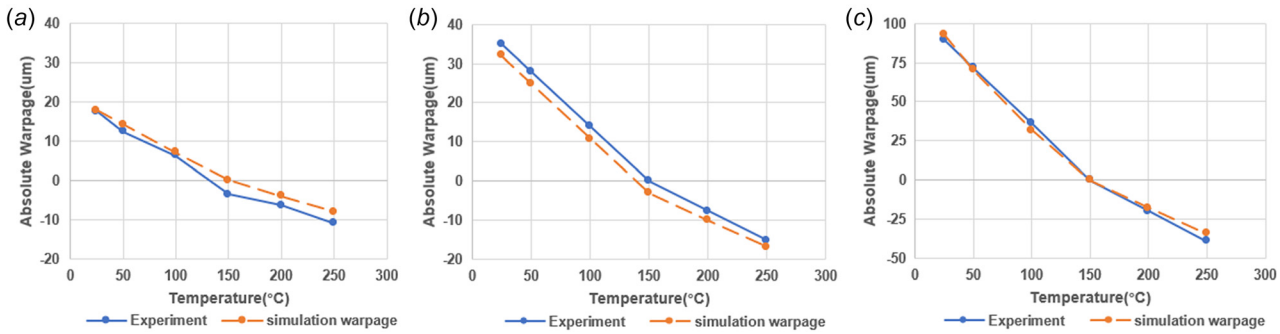

Fig. 17 Warpage comparison between simulation and experiment for t_1–t_3 type B samples: (*a*) 385 μm, (*b*) 275 μm, and (*c*) 170 μm

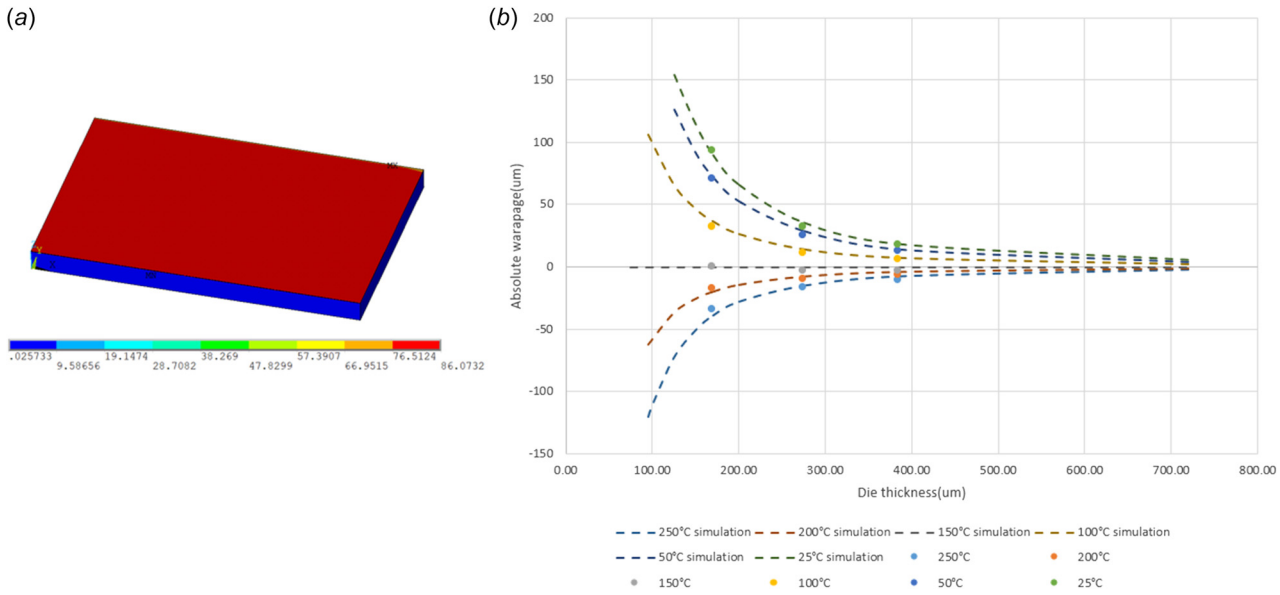

Fig. 18 Type B sample warpage comparison between simulation and experiment: (*a*) stress at room temperature and (*b*) overall comparison between model and all type B samples results

can further predict the chips with other sizes and thicknesses as long as the upper stream process flow is not changed.

Acknowledgment

This paper was presented at the 2023 IEEE 73rd Electronic Components and Technology Conference.

Data Availability Statement

The datasets generated and supporting the findings of this article are obtainable from the corresponding author upon reasonable request.

Nomenclature

CTE = coefficient of thermal expansion
E = Young's modulus
ν = Poisson's ratio
σ = stress

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