# An Analysis of Solder Joint Formation and Self-Alignment of Chip Capacitors

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***Abstract*— An energy-based 3-D model was created to simulate the solder joint formation of the chip capacitor during reflow. The surface tension ($F_s$) and hydrostatic force ($F_h$) of molten solder and the gravitational force ($F_g$) of a chip capacitor and solder paste were considered in this 3-D model. The initial geometry of solder joint is evolved into an equilibrium shape to minimize the internal energy of molten solder. In this study, we investigated the effect of various design parameters, such as solder paste volume, copper pad dimension, and component height on the solder joint shape of capacitor. Chip capacitor C1005 and C0603 with SAC305 solder paste and copper pads with electroless nickel immersion gold (ENIG) surface finish were used as examples. Actual capacitor samples were cross-sectioned and inspected to validate the simulation results from the 3-D model. Moreover, the self-alignment of the chip capacitor was studied in this work. The component self-alignment will affect the accuracy of component assembly and significantly affects the chip capacitor solder joint formation. Simulations were performed to address the mechanism of chip capacitor self-alignment during reflow soldering. The effect of solder paste volume on the capacitor self-alignment was summarized. The result showed relatively more solder paste that can improve the capacitor self-alignment because of the bigger restoring force generated by the molten solder. The inconsistency of solder paste volumes at the two terminations will cause the capacitor to offset from the center. It is found that the misalignment of capacitor C1005 can be reduced to ±30 $\mu$m in component-length direction and ±30 $\mu$m in component-width direction by the optimization of solder paste volume. The self-alignment is better in component-width direction than component-length direction. An extensive number of experimental studies were performed to develop a data-driven prediction model so that the manufacturing cost during trial tests can be reduced. In the experiments, the chip capacitors were placed intentionally with some initial offsets and their positions were measured before and after the reflow. Simulation results showed good agreement with the experimental data.**

***Index Terms*— Chip capacitor, numerical simulation, self-alignment, solder joint shape.**

## I. Introduction

In recent years, electronic devices have increased the demand for miniaturization and more functionalities. However, as the size of the components enters the microstructure domain, big challenges are posed regarding assembly accuracy and reliability. Researchers have found that the reliability of chip components, such as chip capacitors and resistors, is closely related to the solder filet geometry and the standoff height [1]–[5]. Thus, having an in-depth understanding of the component solder joint formation during reflow soldering can help us to optimize the manufacturing parameters and improve the reliability of the components. Thirty-five years ago, Wassink and Verguld [6] created the first 2-D analytical model to calculate the solder joint geometry and explained the tombstoning phenomenon of chip resistors. Later, Heinrich *et al.* [7]–[9] developed a more complex 2-D model to address the effect of solder paste surface tension, density, contact angle, and wetting area on the solder joint geometry of chip components. Jairazbhoy [10] and Rafanelli [11] investigated the effect of solder paste density and volume on the solder filet shape and standoff height of chip components. Wu *et al.* [12] presented a numerical model to simulate the solder joint geometry and predict the tombstoning possibility of surface mount components under different conditions. Researchers have made considerable efforts to analyze the solder joint formation of chip components during reflow. However, the models and calculations of solder joint geometry in previous works are based on many different simplifications and assumptions, which could lead to various discrepancies with the actual solder joint formation.

In this work, an energy-based 3-D model was created using Surface Evolver [13], [14] to simulate the solder joint shape of a chip capacitor in reflow soldering. In this model, the evolution of the solder joint shape is driven by the energy-minimization of the solder paste, and the model fully reflects the behavior of the solder paste during reflow. Solder paste volume, copper pad dimension, chip capacitor termination length, and chip capacitor height as the most important factors in chip capacitor solder joint shape were investigated in this article. We proved that the solder joint shape can be well controlled by adjusting these parameters, which means the most desirable solder joint shape for different purposes can be achieved at the design stage.

Chip capacitor movement during reflow, which is called component self-alignment, can significantly affect the capacitor solder joint shape. Surface mount component self-alignment is driven by the surface tension and hydrostatic force of molten solder. The movement includes in-plane translation, twisting, and tilting, which can eventually change the solder joint shape. Poor self-alignment can cause many common

Manuscript received July 28, 2020; revised October 4, 2020; accepted October 22, 2020. Date of publication October 27, 2020; date of current version January 25, 2021. Recommended for publication by Associate Editor A. Bajwa upon evaluation of reviewers' comments. *(Corresponding author: Seungbae Park.)*

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Digital Object Identifier 10.1109/TCPMT.2020.3034211

assembly defects in industrial production, such as nonwetting, tilting, overhanging, and tombstoning. Thus, a comprehensive understanding of the self-alignment mechanism of the chip capacitor during reflow will help avoid many defects. Many researchers have done extensive studies to analyze the effect of design parameters, such as solder paste type, volume, copper pad shape, dimension, and surface finish, on the self-alignment of chip capacitors [15]–[23]. In this study, we also discuss the effect of solder paste volume regarding capacitor self-alignment. The position of the chip capacitor after reflowing can be predicted by the 3-D model. By applying different solder paste volumes on the two terminations of the chip capacitor, we can address the effect of inconsistent solder paste volumes on self-alignment. The result showed that the capacitor self-alignment in component-length direction was significantly affected by the solder volume inconsistency at the two terminations. And a relatively larger solder paste volume can improve the component self-alignment because of the bigger restoring force generated by the molten solder. Experiments were performed using an automated optical inspection (AOI) machine and a solder paste inspection (SPI) machine to validate the simulation results.

## II. Chip Capacitor Solder Joint Prediction

### A. Energy Minimization Principle

In this work, the energy-based 3-D model was created using the open-source software Surface Evolver. Surface Evolver is a finite element program that minimizes the energy of a surface defined by geometrical and physical constraints. The surface of the solder joint is represented as a simplicial complex that will be divided into many triangular facets. The displacement, force, and energy on each vertex of those triangular facets will be calculated to determine the solder joint shape with minimal energy [14]. The energy minimization is done by evolving the surface down the energy gradient. The solder joint's total internal energy $E_t$, surface energy $E_s$, and the gravitational energy $E_g$ can be calculated by

$$E_t = E_s + E_g; \quad E_s = \int \gamma \, dS; \quad E_g = G * \rho * \iiint z dV.$$

The energy integrals are taken from each facet of the solder joint surface, where $\gamma$, $S$, $\rho$, and $V$ indicate the surface tension coefficient, surface area, density, and volume of molten solder, respectively. $G$ is the gravity constant.

### B. Chip Capacitor Solder Joint Shape Analysis

In this 3-D model, the first step is to define the initial geometry of the chip capacitor, solder joints, and copper pads. Because of the requirement of boundary conditions and constraints of the molten solder, the initial geometry of solder joint is defined as shown in Fig. 1. The solder paste volume ($V_{sp1}$, $V_{sp2}$), copper pad extension length ($L_{pe}$), copper pad width ($W_p$), capacitor termination length ($L_t$), and capacitor height ($H_c$), which are the predominant factors in chip capacitor solder joint shape, are discussed in this article. Eutectic solder paste SAC305, which is the most popular solder paste in industrial practice, is chosen for this study.

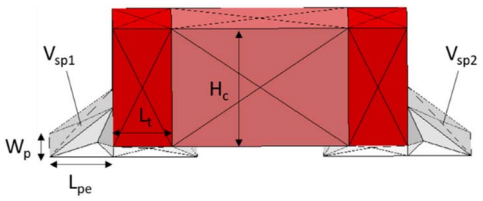


Fig. 1. User-defined initial geometry of a chip capacitor and solder joint.

TABLE I
Specifications of Chip Capacitors and Copper Pad

| | C1005 | C0603 | C0402 |
|---|---|---|---|
| Dimension (cm) LxWxH | 0.1x0.05x0.042 | 0.06x0.03x0.023 | 0.04x0.02x0.013 |
| Weight (mg) | 1.6 | 0.33 | 0.09 |
| Termination length (cm) | 0.02 | 0.015 | 0.01 |
| Recommended solder paste volume ($cm^3$) | $2.85\times10^{-5}$ | $7.77\times10^{-6}$ | $3.29\times10^{-6}$ |
| Pad dimension LxW (cm) | 0.05×0.056 | 0.03×0.034 | 0.02×0.022 |
| Pad-to-pad distance (cm) | 0.048 | 0.030 | 0.016 |


Fig. 2. SAC305 solder paste contact angle measurement.

Its surface tension is 544.9 dyn/cm [16], and its density is 7.361 g/$cm^3$. The contact angle of SAC305 solder paste on an electroless nickel immersion gold (ENIG) surface finished copper pad is measured to be 24° by the static sessile drop test in a nitrogen environment (Fig. 2). The commercial chip capacitors C1005, C0603, and C0402 are used as examples in this study, and their specifications are listed in Table I. We assume the molten solder does not overspread the wetting area during reflow because it is fully constrained by the solder mask. The resin curing effect, chemical reaction between solder and copper pad, and oxidation of solder paste during reflow are not considered in this model [24]–[26].

To address the effect of solder paste volume on chip capacitor solder joint shape, simulations were performed using capacitors with different solder paste volumes. Here, we set the solder paste volume recommended by the manufacturer to be 100%. And the solder joint geometries of the chip capacitor C1005 with solder paste volume $V_{sp1}/V_{sp2}$ (50%/50%, 100%/100%, and 150%/150%) were simulated using our 3-D model [Figs. 1 and 3(1)]. In this simulation, the capacitor is fixed in the middle of two copper pads. Therefore, we do not complicate the problem by introducing the effect of capacitor in-plane movement. The chip capacitor can move vertically, and the standoff height can be predicted from solder paste volumes. Fig. 3(1) shows that when we increase the solder

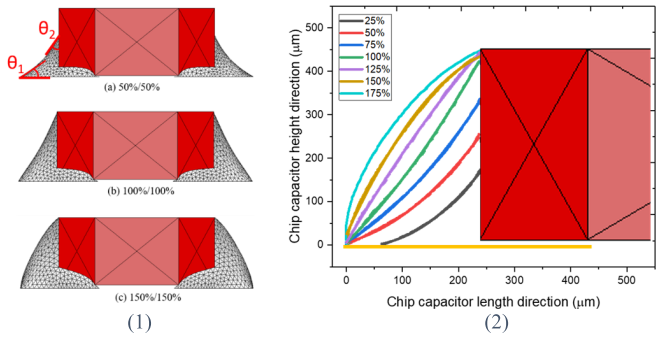


Fig. 3. (1) Solder joint geometry of capacitor C1005. (2) Chip capacitor solder joint filet profiles.

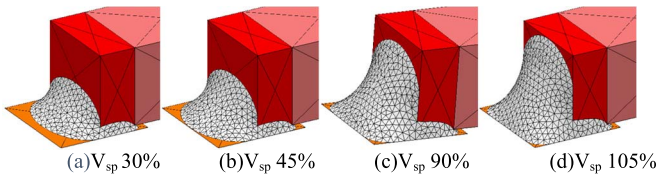


Fig. 4. Wetting of molten solder on copper pad. (a) Stage A, molten solder spreads freely on the copper pad. (b) Stage B, molten solder reaches the left edge of the copper pad. (c) Stage C, molten solder is fully constrained by the edge of the copper pad. (d) Stage D, the molten solder reaches the top edge of the capacitor sidewall.

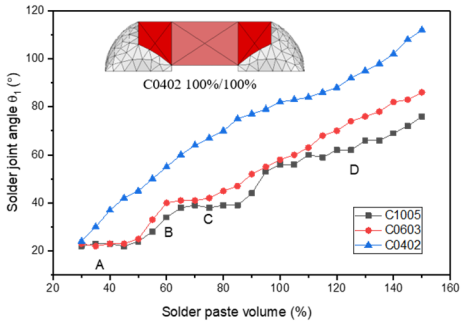


Fig. 5. Capacitor solder joint angle $\theta_1$ with different solder paste volumes.

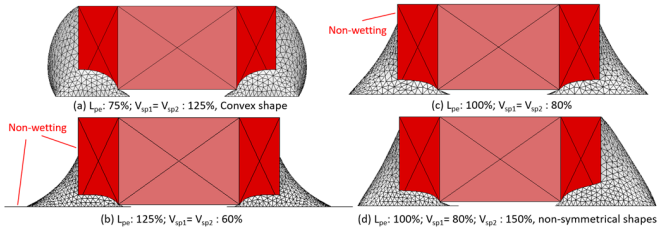


Fig. 6. Four types of imperfect solder joint shapes. (a) $L_{pe}$: 75%; $V_{sp1} = V_{sp2}$: 125%, convex shape. (b) $L_{pe}$: 125%; $V_{sp1} = V_{sp2}$: 60%. (c) $L_{pe}$: 100%; $V_{sp1} = V_{sp2}$: 80%. (d) $L_{pe}$: 100%; $V_{sp1} = 80\%$; $V_{sp2}$: 150%, nonsymmetrical shapes.

paste volume from 50% to 150%, the solder joint shape will change gradually from concave to convex. Our research can provide manufacturers with good guidelines on the solder paste volume design to achieve the most desirable solder joint shape according to their needs. For instance, the solder joint filet close to a straight line is preferred by the electronic packing industry [Fig. 3(1b)]. The relationships between the solder joint filet profile and solder paste volume are summarized in Fig. 3(2). When the solder paste volume is small, the molten solder has enough space to spread freely on the copper pad in a horizontal direction and along the sidewall of the capacitor in a vertical direction, which is denoted by Fig. 4(a). Thus, the solder joint angle $\theta_1$ can maintain the contact angle (24°) of SAC305 molten solder, and the solder joint will always be a concave shape. However, when we increase the volume until the molten solder reaches the edge of the copper pad [Fig. 4(b)], $\theta_1$ will start to increase. The transition from concave shape to convex shape will occur. Thus, the solder joint angle $\theta_1$ can be a good indicator of the capacitor solder joint shape. In Fig. 5, the solder joint angle $\theta_1$ of three types of capacitors is plotted as a function of solder paste volume. The change of the solder joint angle occurs in four stages (A, B, C, and D). As explained, $\theta_1$ maintains about 24° in stage A because the molten solder can spread freely. And $\theta_1$ starts to increase when the molten solder reaches the edge of the copper pad, which is stage B [Fig. 4(b)]. In stage C, the molten solder is fully contacting the edge of the copper pad, so the $\theta_1$ will be temporarily stable [Fig. 4(c)]. But the molten solder still spreads along the sidewall of the capacitor. When the molten solder reaches the top edge of the capacitor sidewall, $\theta_1$ will start to increase again, which is stage D. The solder joint angle $\theta_1$ of capacitors C1005 and C0603 has a similar tendency, but capacitor C0402 shows a different result. The solder paste volume recommended by the manufacturer for capacitor C0402 is too large for its copper pad and component height. Therefore, it only shows the stage D of capacitor C0402. By recognizing the mechanism of molten solder wetting, we can better understand the solder joint formation during reflow.

Along with solder paste volume ($V_{sp}$), the copper pad extension length ($L_{pe}$) plays an important role in the solder joint shape of a chip capacitor. For instance, the complete-wetted capacitor solder joint with a straight solder joint filet is said to have a desirable solder joint shape in some electronic devices [Fig. 3(1b)]. However, improper combinations of $V_{sp}$ and $L_{pe}$ will cause four types of imperfect solder joint shapes (Fig. 6). Therefore, to obtain a desirable solder joint shape, we should select the proper $V_{sp}$ and $L_{pe}$ based on the size of the chip capacitor. Theoretically, there are an infinite number of combinations of $V_{sp}$ and $L_{pe}$ that can achieve good solder joint shape for each specific chip capacitor (Table II, Fig. 7). Combinations with bigger $V_{sp}$ and longer $L_{pe}$ can produce solder joints with better mechanical reliability when the chip capacitor undergoes vibration or impact. While combinations with smaller $V_{sp}$ and shorter $L_{pe}$ can produce a finer component pitch so that the board density can be increased. Hence, the proper combination of $V_{sp}$ and $L_{pe}$ should be selected for different applications to have a balance between the mechanical reliability and board density.

Experiments validated the simulation results from our 3-D model. Different solder paste volumes $V_{sp1}/V_{sp2}$ (51%/50%, 80%/79%, and 130%/134%) were applied to solder the capacitor C1005 on the test printed circuit board (PCB), and their solder joint filet profiles were inspected by the AOI machine

TABLE II
INPUT VALUES OF $L_{pe}$ AND $V_{sp}$ IN THE SIMULATIONS

| | $L_{pe}$ (μm) | $L_{pe}$ (%) | $V_{sp}$ (μm$^3$) | $V_{sp}$ (%) |
|---|---|---|---|---|
| Case 1 | 140 | 58.3 | 2.14x10$^7$ | 75 |
| Case 2 | 165 | 68.8 | 2.34x10$^7$ | 82 |
| Case 3 | 190 | 79.2 | 2.57x10$^7$ | 90 |
| Case 4 | 240 | 100 | 3.08x10$^7$ | 108 |
| Case 5 | 265 | 110.4 | 3.36x10$^7$ | 118 |
| Case 6 | 290 | 120.8 | 3.82x10$^7$ | 134 |

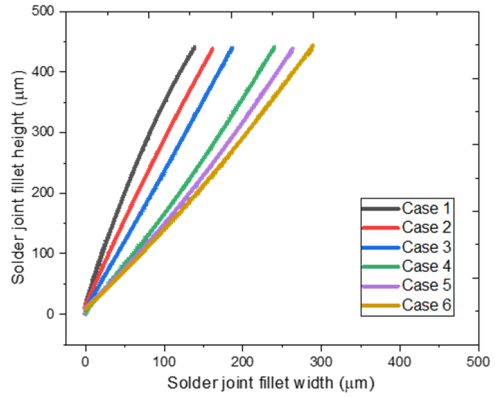


Fig. 7. Solder joint filet profiles for chip capacitors.

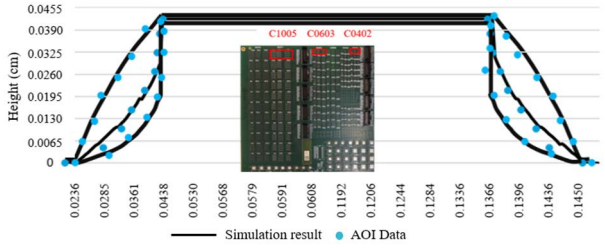


Fig. 8. Solder joint profile of capacitor C1005 from simulation and AOI inspection.

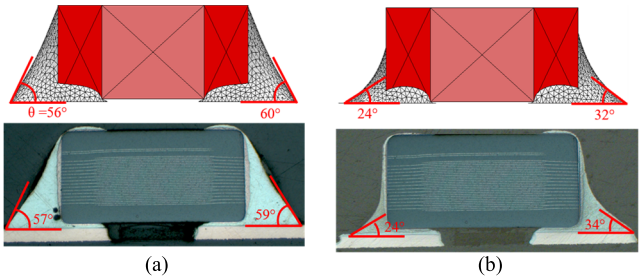


Fig. 9. Comparison between predicted solder joint shape and sample cross section of capacitor C1005: (a) $V_{sp1} = 101\%$, $V_{sp2} = 103\%$ and (b) $V_{sp1} = 50\%$, $V_{sp2} = 74\%$.

after reflow. The AOI data showed good correlation to the solder joint profile predicted by the 3-D model (Fig. 8). Moreover, numerous chip capacitor samples were cross-sectioned and compared with the simulation results to confirm the reliability of the model. In Fig. 9, there are two examples

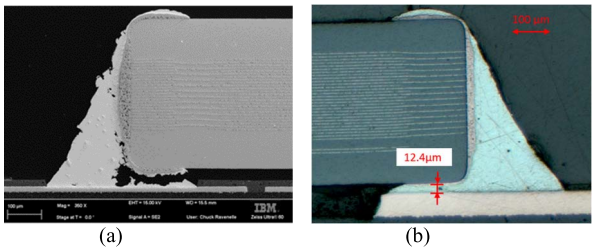


Fig. 10. (a) Crack initiates from the bottom of the capacitor [27]. (b) Standoff height of capacitor C1005 with $V_{sp}$ 105%.

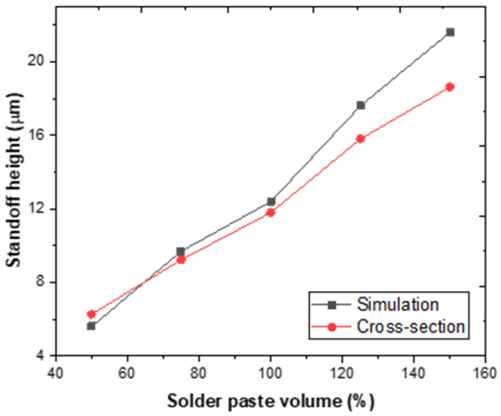


Fig. 11. Standoff height of capacitor C1005 with respect to $V_{sp}$.

of chip capacitor C1005 with different solder paste volumes. The solder joint shapes predicted by our model present good agreement with the actual sample cross sections.

### C. Solder Joint Standoff Height Prediction

As discussed in many studies, the solder joint standoff height is closely related to the fatigue life of a chip capacitor [4], [5]. When the chip capacitor starts to fail under thermal loading, the crack tends to initiate from the solder underneath the component because of the shear stress generated by the coefficient of thermal expansion (CTE) mismatch between the chip and the substrate [Fig. 10(a)] [4], [27]–[29]. Fortunately, the shear stress concentrates at the solder joint but can be reduced by increasing the standoff height. This study found that the solder paste volume ($V_{sp}$) and the termination length can significantly affect the standoff height of the chip capacitor. Simulations are performed to predict the standoff height of the C1005 with the recommended copper pad dimension but different $V_{sp}$. The results show that standoff height can be effectively increased by adding more solder paste (Fig. 11). More than 40 samples were cross-sectioned, and their standoff heights were measured to validate the simulation results. The chemical reaction between the molten solder and copper pad was not considered in the simulation, which can introduce some discrepancies between the simulation and cross section results. Fig. 10(b) shows an example of the capacitor C1005 cross section with 105% $V_{sp}$, and its standoff height is around 12.4 $\mu$m.

The effect of capacitor termination length ($L_t$), which is the tin-plated area (Fig. 1), on the solder joint standoff height is studied. Chip capacitor C1005 with 100% $V_{sp}$ and the

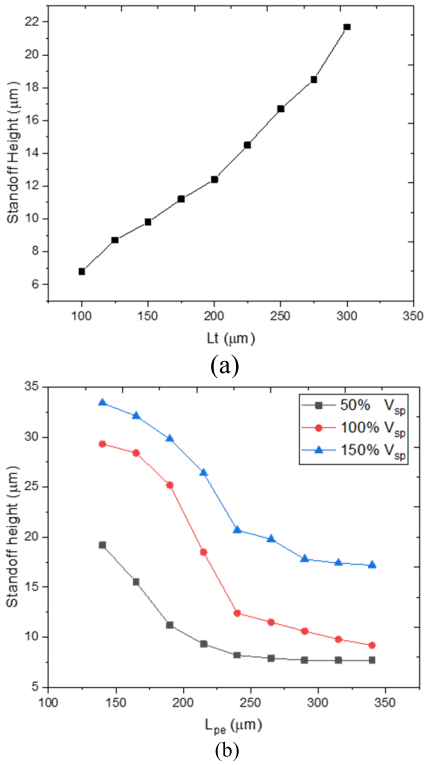


Fig. 12. (a) Standoff height of capacitor C1005 with respect to $L_t$. (b) Standoff height of capacitor C1005 with respect to $L_{pe}$.

recommended copper pad size are used in the model. The capacitor termination length, $L_t$, applied in this simulation ranges from 100 to 200 $\mu$m (50%–150%). The results show that the standoff height of C1005 increases with the termination length, $L_t$ [Fig. 12(a)]. The effect of the pad extension length $L_{pe}$ on the standoff height was also investigated. Similarly, we can also obtain higher standoff height by controlling $L_{pe}$ with $V_{sp}$ remaining constant [Fig. 12(b)]. In summary, a certain standoff height can be obtained by adopting proper $V_{sp}$, $L_t$, and $L_{pe}$. Even though there are standards in IPC and JEDEC for these parameters, different companies make slight adjustments according to their needs. Hence, the analysis of capacitor solder joint formation can be used as a guide for the rational design of capacitor solder joints.

## III. Chip Capacitor Self-Alignment

### A. In-Plane Translation Self-Alignment

In Section II, we assume the chip capacitor can only move in the vertical direction in the simulations, so that we do not mix the effect of the solder paste volume and capacitor in-plane movement on the solder joint shape of the chip capacitor. However, the chip capacitor repositions itself during real reflow in the molten solder in ways that include in-plane translation, twisting and tilting, a process referred to as the self-alignment of the chip capacitor. Poor self-alignment can cause many assembly defects in an industrial production, such as nonwetting, tilting, overhanging, bridging, and tombstoning. Therefore, a comprehensive study on the mechanism of self-alignment is the cornerstone of improving the self-alignment of chip components during reflow. In this study, the effect of solder paste volume on the in-plane translation

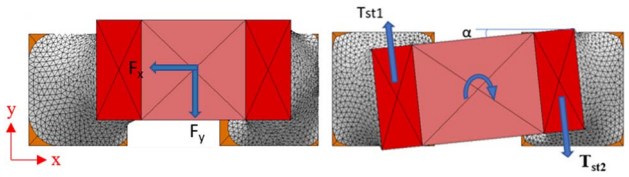


Fig. 13. Restoring force and torque schematic of chip capacitor during reflow.

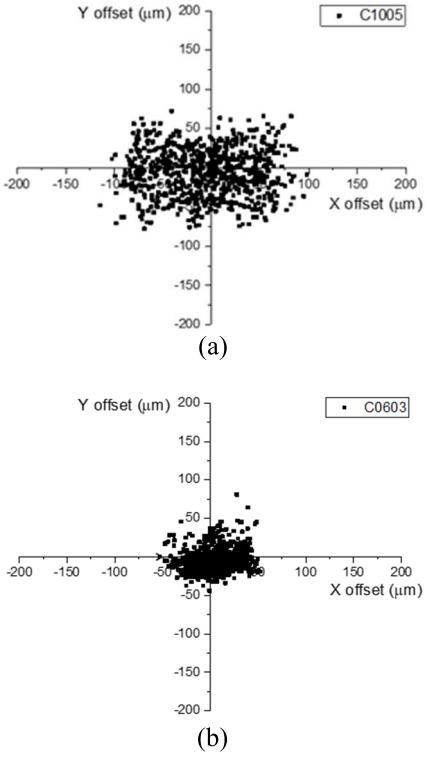


Fig. 14. $x$ and $y$ offset of the capacitors after reflow: (a) capacitor C1005 and (b) capacitor C0603.

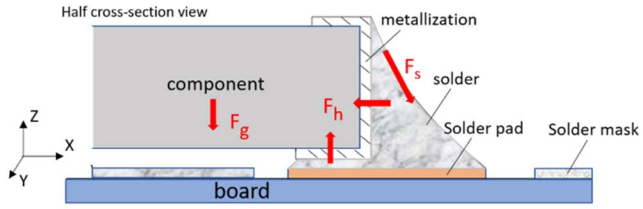


Fig. 15. Force schematic of chip capacitor during reflow.

self-alignment and twisting self-alignment (Fig. 13) were investigated. 700 C1005 capacitors and 700 C0603 capacitors were placed on the test PCB and then went through reflow process to quantify the misalignment of these two types of capacitor. The result shows that the misalignment of C1005 is $\pm 100$ $\mu$m in the $x$-direction and $\pm 50$ $\mu$m in the $y$-direction [Fig. 14(a)]. As for capacitor C0603, the misalignment in the $x$-direction is $\pm 50$ $\mu$m, and $\pm 40$ $\mu$m in the $y$-direction [Fig. 14(b)]. Except from the placement tolerance of the capacitor placement machine, it is believed that the inconsistence of the solder paste volume at the two terminations of the capacitor can also significantly affect the self-alignment accuracy of these capacitor, which is the focus of this study.

In this 3-D model, the surface tension and hydrostatic force of molten solder and the gravitational force of the

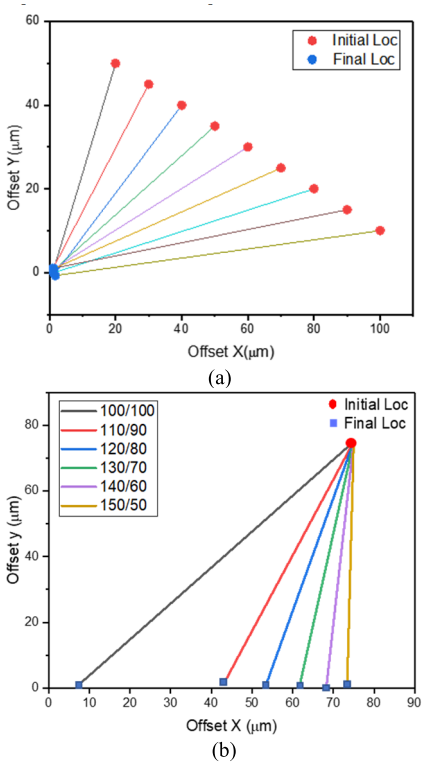


Fig. 16. Capacitor C1005 in-plane translation self-alignment. (a) $V_{sp1} = V_{sp2}$. (b) $V_{sp1} \neq V_{sp2}$.

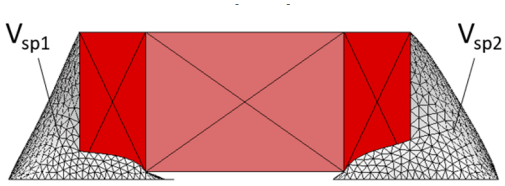


Fig. 17. Capacitor shifts from the middle of two copper pads to the left side, when $V_{sp1} < V_{sp2}$.

chip capacitor and solder paste were considered (Fig. 15). The resulting restoring force, $F$, and restoring torque, $T$, are calculated based on the principle of virtual work

$$F = -\frac{E(q+\delta q) - E(q-\delta q)}{2 * \delta q}$$

$$T = -\frac{E(\theta+\delta\theta) - E(\theta-\delta\theta)}{2 * \delta\theta}.$$

The simulation results show that perfect self-alignment can be achieved if $V_{sp1}$ equals $V_{sp2}$, regardless whether the capacitor is initially misplaced [Fig. 16(a)]. However, because of the precision limit of the solder paste control system, $V_{sp1}$ is usually slightly different from $V_{sp2}$, which can cause a component to offset after reflow. Simulations are performed to investigate the capacitor in-plane shifting self-alignment with different combinations of $V_{sp1}$ and $V_{sp2}$ [Fig. 16(b)]. Large capacitor offsets in the $x$-direction are observed when $V_{sp1}$ is different from $V_{sp2}$, while self-alignment in the $y$-direction is not affected by inequality of $V_{sp1}$ and $V_{sp2}$. The example in Fig. 17 shows the capacitor shifts 26.3 $\mu$m away from the center of two copper pads when $V_{sp1}$ is 100% and $V_{sp2}$ is 150%.

To validate our self-alignment prediction model, a capacitor C1005 and a capacitor C0603 were mounted on the test PCB

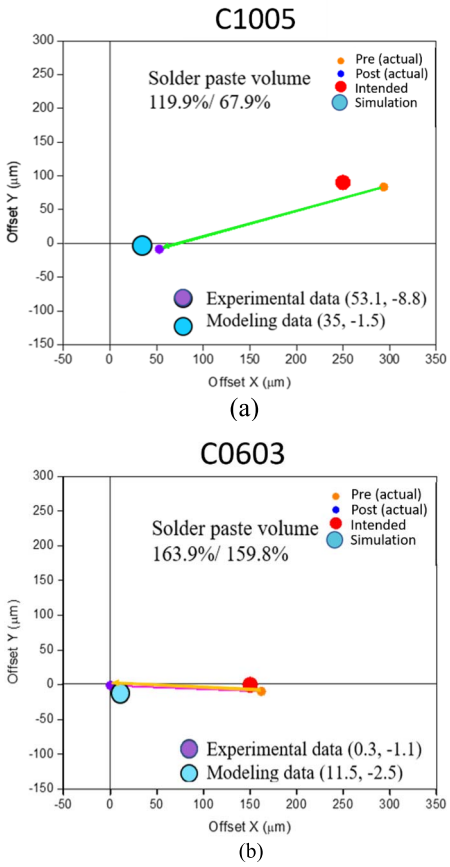


Fig. 18. Self-alignment result comparison between experiment and model prediction: (a) self-alignment results of capacitor C1005 and (b) self-alignment results of capacitor C0603. Pre: the initial location of the capacitor. Post: the location of the capacitor after reflow. Intended: the designed location of the capacitor. Simulation: the location of capacitor predicted by the 3-D model.

as examples, and their positions were recorded before and after reflow, using the AOI machine. The results showed the capacitor's initial location was off from the designed location because of a placement error. However, because of the restoring force from the molten solder, the capacitors can self-align and improve the assembly accuracy (Fig. 18). Simulations were performed under the same conditions. The predicted location of capacitor C1005 was 18 $\mu$m off in the $x$-direction from the experiment data, and it was 6.3 $\mu$m off in the $y$-direction from the experiment data [Fig. 18(a)]. This discrepancy is believed to be introduced by the simplifications and assumptions of our 3-D model, which will be further studied in the future. The component self-alignment in the $y$-direction tended to be better than the self-alignment in the $x$-direction.

To explain the difference of self-alignment performance in the $x$- and $y$-directions, the restoring forces in those directions during reflow were calculated and plotted (Fig. 19). When the offset is within 30 $\mu$m, the restoring force in the $x$-direction is too small to move the capacitor. However, the restoring force in the $y$-direction is much bigger than in the $x$-direction, which makes better self-alignment in the $y$-direction. In Fig. 20, this force schematic describes the directions of the restoring force from the molten solder at the two terminations of the capacitor. When the capacitor is close to the center of the two copper pads, the $x$ component of restoring force $F_{st1}$ and $F_{st2}$ are in

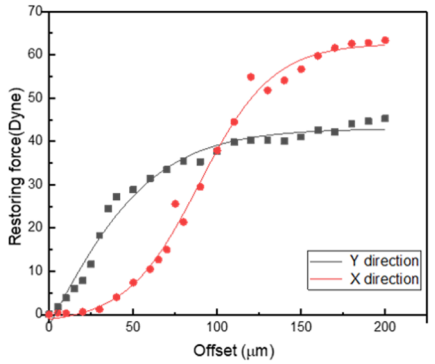


Fig. 19. Restoring force of capacitor C1005 in $x$- and $y$-directions with 100%/100% $V_{sp}$.

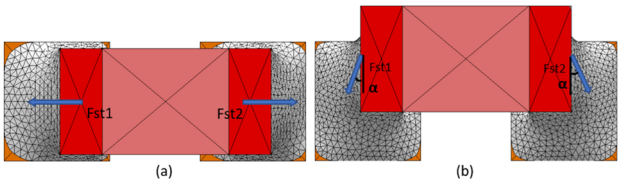


Fig. 20. Force schematic of the chip capacitor during reflow. (a) Capacitor is off in $x$-direction. (b) Capacitor is off in $y$-direction.

opposite directions. While the $y$ component of $F_{st1}$ and $F_{st2}$ is always toward the same direction, which results in bigger restoring force in the $y$-direction within a certain range.

### *B. In-Plane Twisting Self-Alignment*

In industrial practice, the twisting misplacement (Fig. 13) is a concern in surface mount assemblies. In this study, the effect of solder paste volume on capacitor twisting self-alignment is investigated. In the simulation, we intentionally rotated the capacitor with an angle $\alpha$ (10°) and calculated the restoring torque using the virtual work method. First, $V_{sp1}$ and $V_{sp2}$ were set to different amounts, but the sum of $V_{sp1}$ and $V_{sp2}$ was kept a constant 200%. In this case, no significant difference was observed in the restoring torque results (Fig. 21). However, when we gradually increased the sum of $V_{sp1}$ and $V_{sp2}$ from 100% to 300% ($V_{sp1} = V_{sp2}$), the results showed that the total restoring torque will increase when more solder paste was applied (Fig. 22). The capacitor's twisting self-alignment will not be affected by an inequality of $V_{sp1}$ and $V_{sp2}$. Instead, it will be significantly affected by the total amount of solder paste that is applied. Thus, relatively more solder paste will be helpful to improve the capacitor twisting self-alignment during reflow.

## IV. Conclusion

In this study, an energy-based 3-D model was created to predict the solder joint shape and self-alignment during reflow. The effects of solder paste volume on the solder joint shape and self-alignment are addressed. We proved that the solder joint shape of the capacitor can be well controlled by choosing different combinations of solder paste volume ($V_{sp1}$, $V_{sp2}$) and copper pad extension length ($L_{pe}$), which can guide the manufacturers to optimize the solder paste volume for different surface mount components. Actual sample cross sections were inspected to validate the results from the model. Moreover, this 3-D model is a powerful tool to predict the capacitor self-alignment performance at different combinations of solder paste volume $V_{sp1}$ and $V_{sp2}$. The capacitor tends to self-align better in the component-width direction ($y$) than component-length direction ($x$), which can be explained by the restoring force in the $x$- and $y$-directions. Capacitor twisting self-alignment is not affected by an unequal $V_{sp1}$ and $V_{sp2}$. Instead, the total amount of solder paste will significantly affect the twisting self-alignment of the capacitor. Because of the flexibility of this 3-D model, it can be used for capacitors and applied to other surface mount components.

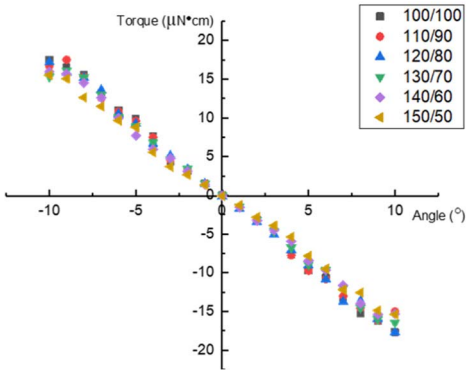


Fig. 21. Total restoring torque when $V_{sp1} \neq V_{sp2}$.

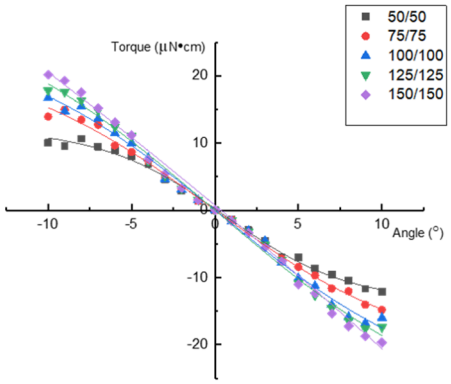


Fig. 22. Total restoring torque when $V_{sp1} = V_{sp2}$.

## Acknowledgment

The authors would like to thank all the laboratory members from Opto-Mechanical and Physical Reliability Laboratory, Prof. Sang Won Yoon and Prof. Daehan Won of Systems Science and Industrial Engineering (SSIE) Department for their support on this project.

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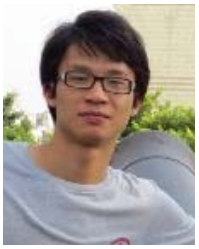

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