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Design guideline on board-level thermomechanical reliability of 2.5D package

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ABSTRACT

A vast range of electronics products have utilized 2.5D packages for better performance and miniaturization. As multi-level assembly technologies are getting mature, 2.5D packaging technology becomes affordable. In this work, design guideline for board-level reliability of a 2.5D package was provided with respect to accelerated thermal cycling (ATC) and power cycling (PC). Finite element models were built and validated step-by-step by warpage measurement. Solder fatigue life in power cycling was investigated with temperature mapping technique merged into the process of scripting, which conducts load transfers from computational fluid dynamics (CFD) simulation to finite element analysis (FEA). ATC test was conducted with solder joint failure analysis. Fatigue life projection model was determined by correlation between tested life data and simulation results. Parametric studies regarding geometry factors and material properties were performed including PCB, substrate, thermal interface material (TIM) and lid adhesive, to give design suggestions to improve board-level thermal reliability. It is found that CTE mismatch between the substrate and the PCB is the major factor affecting board-level reliability in accelerated thermal cycling. Maximum junction temperature of a 2.5D FPGA package is dependent on application scenarios and working environment. Designed maximum junction temperature and applied heatsink clamping force have considerable influences on board-level reliability.

1. Introduction

The concept of housing multiple dies in a shared package has always been attractive to engineers, to achieve reduced interconnect length, integrated functions, reduced overall form factors, and enhanced performance. Currently, a 2.5D package is typically defined as multiple dies being placed side by side in a single package [1]. The distinguishing features of 2.5D packages include 1) homogeneous or heterogenous multiple dies, 2) microbump interconnect and 3) a passive interposer. Microbump interconnect can be realized by using solder bumps, Cu pillars or Cu-to-Cu bonding technology. The interposer is fabricated with in-plane fine-line metallization layers for die-to-die interconnect. 2.5D integration has many advantages over previously-designed multi-chip modules and hybrid modules [2]. It provides a smaller footprint, increased reliability, higher power utilization efficiency and enhanced electrical performance. Furthermore, 2.5D integration becomes affordable because of Though-Silicon-Via (TSV) technology and multi-level assembly technology.

Solder fatigue damage can be accumulated at various types of loading conditions including mechanical loading, thermal cycling, thermal shock, vibration etc. Solder alloys may exhibit inelastic deformation and creep behavior depending on stress and temperature. Fatigue failures caused by excessive creep deformation are predominant in Accelerated Thermal Cycling (ATC) test and Power Cycling (PC) test [3,4]. ATC test and PC test have been widely adopted for evaluating board-level reliability of electronic assemblies [5]. However, during the fast update of products, time cost of these test methods become crucial, increasing product development time and putting constraints on design optimization [6].

To overcome this limitation, an alternative way is to develop a solder fatigue life projection method based on simulation and tested life data, which can provide reasonable and fast life predictions. It is beneficial and even necessary during design phase of electronic products. There are many research work studying life projection models of solder interconnect in the past decade [7,8]. Various physical variables related to solder were used as solder damage indices, including stress, inelastic strain, creep strain and inelastic energy [8]. Darveaux [9,10] developed an energy-based life projection model dividing the entire fatigue life

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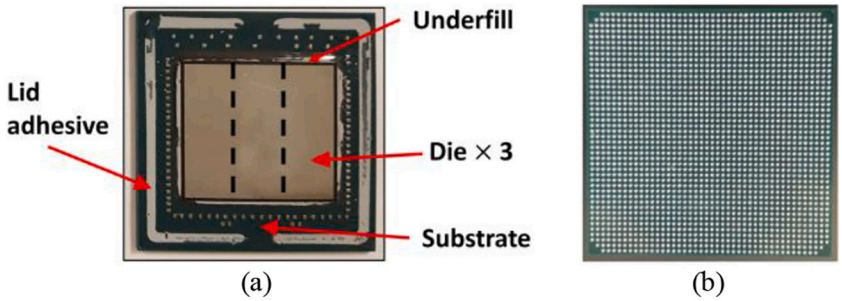

Fig. 1. (a) Image of the 2.5D package with lid removed. (b) Image of the 2.5D package on the BGA side.

Table 1
Geometry parameters.

Item	Dimension	Item	Dimensions
Lid size	55 × 55 × 0.8 mm^3	Substrate size	55 × 55 × 1.8 mm^3
PCB size	383 × 140 × 3.4 mm^3	Lid attach thickness	0.11 mm
Lid stiffener thickness	0.7 mm	BGA ball diameter	0.6 mm
BGA pitch	1 mm	BGA ball height	0.4 mm
Pad diameter	0.63 mm	Diameter of pad solder mask opening	0.53 mm

into two stages, crack initiation stage and crack propagation stage. It is one of the most popular solder fatigue models that have been adopted. Syed [11] developed a lumped solder fatigue life projection model for SnAgCu solders, using one fitting constant to predict fatigue lives of various ball-grid-array assemblies with difference dimensions and structures.

For power cycling simulation, sequentially-coupling technique was implemented in previous studies for thermal and structural analysis. BGA assemblies with eutectic solder under ATC and PC were studied by Darveaux [9,10,12] and Mawer [13] via experiment and simulation. Hong et al. [14] performed power cycling test and simulation showing different failure behaviors between PC and ATC. Subbarayan [15–17] had extensive experimental and numerical work on PC simulation techniques and comparison between ATC and PC, demonstrating that PC and ATC are equivalent and both are able to represent failure in the field. In sequentially-coupling technique, transient heat transfer coefficients (HTC) on surfaces of the geometry are solved first via computational fluid dynamics (CFD), with the presence of cooling liquid (e.g. air, water, etc.). Then, these HTCs are applied onto a finite element model, which shares the same geometry, as boundary conditions. The nonuniform distributed temperature field is solved again and the corresponding stresses and strains are obtained. One disadvantage of this technique is that the simulation results depend on the difference between FEA results and CFD results with respect to the temperature field. Also, high temperature gradient is hard to capture if one HTC value is simply used to represent an entire surface. One way to reduce the difference is to divide the surfaces into smaller areas generating multiple HTCs, which yet brings more uncertainties and increases the time cost of modeling.

Through-silicon interposers are typically utilized in 2.5D packages for high-end applications (e.g. Graphics Processing Unit, Field-Programmable Gate Array), which have large and thick chips and high power densities [1]. Thus, thermal management and thermo-mechanical reliability are critical for designing 2.5D packages [18]. There are numerous studies on stress reduction in low-k interlayer dielectric [18–20] and package-level warpage control [18,21,22] for thermo-mechanical reliability. This paper is focused on board-level reliability of 2.5D packages, and the effect of nonuniform temperature distribution over large interposers during power cycling.

In this work, a design guideline was provided for a 2.5D package to improve board-level reliability in thermal cycling and power cycling. Step-by-step model validation for finite element analysis was performed using warpage measurement. For the first time, a temperature mapping technique was used in power cycling simulation for life prediction in the area of electronic packaging. Power cycling simulation results present the effect of junction temperature and heat sink clamping force on solder fatigue life.

The reminder of this paper is organized as follows. In Section 2, finite element modeling is presented for a 2.5D package in accelerated thermal cycling. Three-step model validation by warpage measurement data is presented. In Section 3 a thermal-fluid-structure simulation methodology for power cycling is introduced, including temperature mapping technique and mapping quality check. The test method and test results of accelerated thermal cycling are presented in Section 4. Based on the tested life data, solder fatigue life projection model and life prediction are presented in Section 5. Also, a design guideline for the board-level reliability of the 2.5D package is provided based on parametric study in this chapter.

2. Accelerated thermal cycling simulation

2.1. Package specification

The 2.5D package is shown in Fig. 1. This 2.5D package consists of an organic substrate, an interposer, three silicon dies and a metal lid. The interposer is mounted on the substrate with Controlled Collapse Chip Connection (C4) interconnects. Three dies are connected to the top surface of the interposer with micro-bump interconnects. The lid is attached on the substrate using lid adhesive. The dimensions of the sample are listed in Table 1. The gap distance between dies is 40 μm. The structure illustration and the cross-section image are shown in Fig. 2.

The surface finish of substrate on the BGA side is Organic Solderability Preservatives (OSP) with Solder Mask Defined (SMD) copper pads. The 28-layer PCB has also the OSP surface finish. Its copper pad is Non-Solder Mask Defined (NSMD). The solder alloy is SAC305 (96.5%Sn-3.0%Ag-0.5%Cu).

2.2. Finite element model

A 3D quarter-symmetry board-level finite element model was built (Fig. 3). Warpage of assembly and accumulated inelastic work in critical solder joint are obtained from simulation. The temperature range of ATC is between 0 °C and 100 °C, with 40-min cycle time (ramp rate is 10 °C/min and dwell time is 10 min). The reference temperature (stress-free) is assumed as 100 °C in this study. The dimensions in simulation model follow Table 1. The boundary conditions are illustrated in Fig. 4.

3D digital image correlation (DIC) was utilized to characterize CTE of PCB and substrate in this study. DIC, which is a form of photogrammetry, is a noncontact and full-field optical measurement technique in which both the in-plane and the out-of-plane deformation can

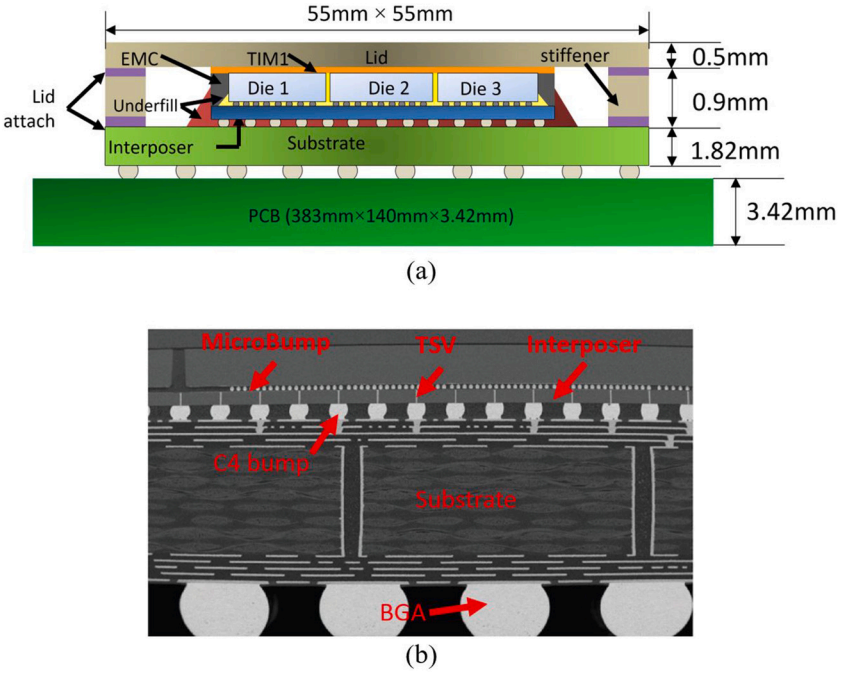

Fig. 2. Structure of the 2.5D package with silicon interposer. (a) Illustration. (b) Image of the cross section showing detailed features: microbumps, C4 bumps and TSVs.

be recognized by correlating the successive images of samples at the initial and the deformed status [23-25]. The field of view (FOV) size is $72 \times 60\,mm^2$ in this study. The empirical sensitivity of displacement measurement of DIC system can be calculated as FOV/30000 [26], which is $\pm 2.4\,\mu m$. The CTE was determined by computing the slope in the plot of strain versus temperature. Figs. 5(a) and 6(a) present the CTE measurement data.

The moduli of PCB and substrate were measured by Dynamic Mechanical Analysis (DMA) system. The measurement results are shown in Figs. 5(b) and 6(b). The PCB or substrate was diced into a size

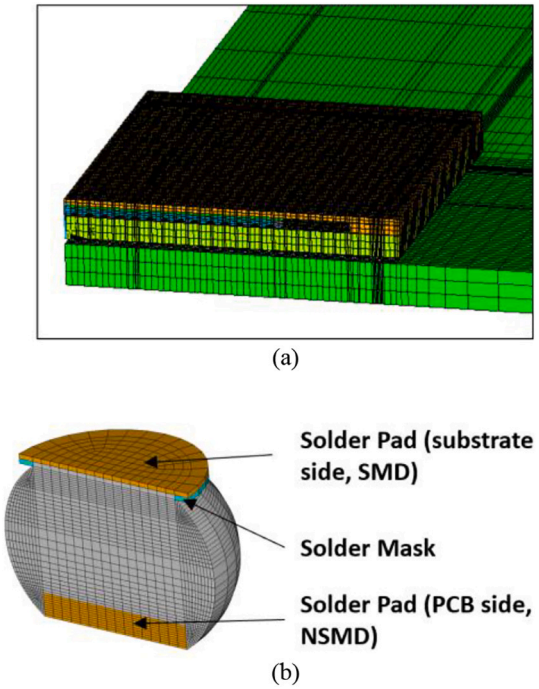

Fig. 3. (a) Finite element model of the 2.5D package mounted on PCB. (b) Mesh in the critical solder joint with solder mask and pads.

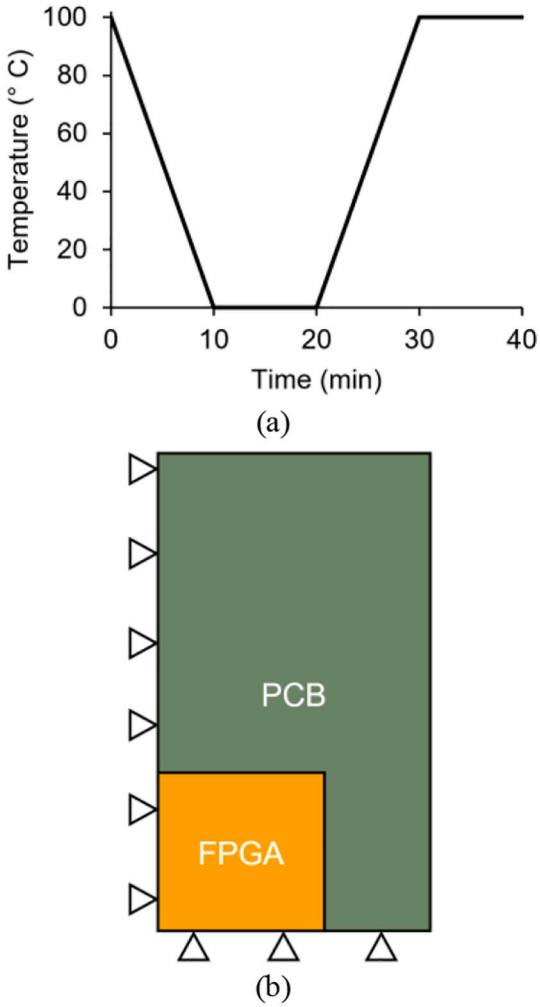

Fig. 4. Boundary conditions of finite element model for ATC. (a) Temperature condition; (b) Quarter-symmetry boundary condition.

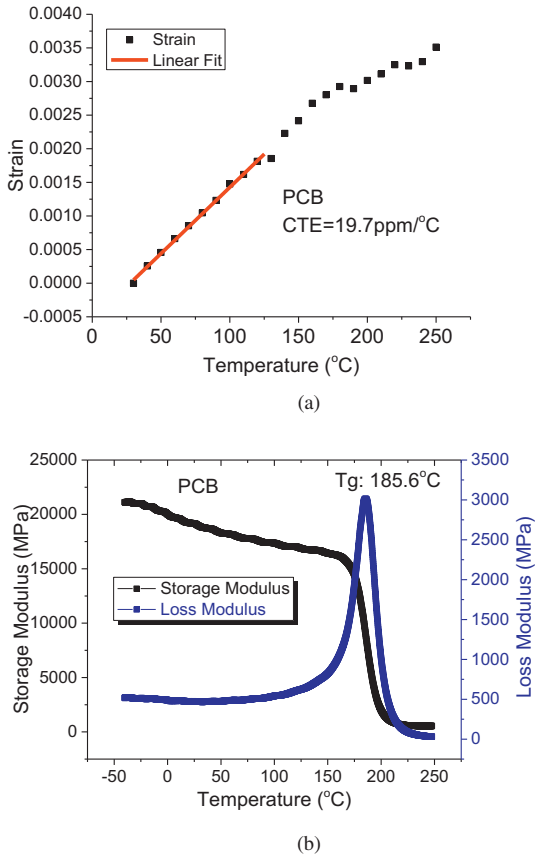

Fig. 5. Measurement results for material characterization of PCB. (a) CTE. (b) Modulus.

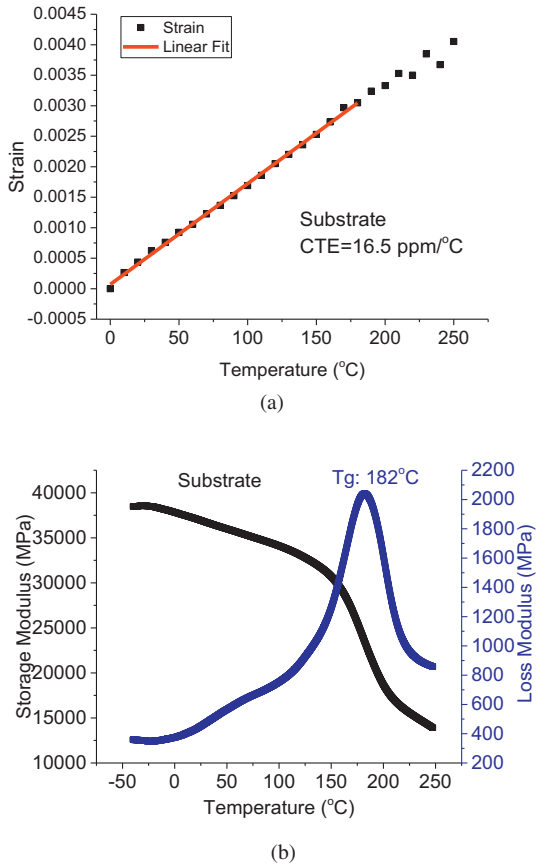

Fig. 6. Measurement results for material characterization of substrate. (a) CTE. (b) Modulus.

of 20 × 3.8 × 1.2 mm^3 and 0.1% strain was induced with 1 Hz loading frequency in three-point bending tests. The storage modulus from DMA test data was extracted as the temperature-dependent elastic modulus.

Other material properties are listed in Table 2. A rate-dependent constitutive model, Anand model with 9 constants was applied to characterize the inelastic behavior of SAC305 solder alloy [4]. The model parameters are listed in Table 3.

The structures of C4 bump and micro-bump interconnect, are illustrated in Fig. 7. In this work they are simplified as isotropic layers. The effective material properties (modulus, CTE and Poisson's ratio) for this layer were calculated using rule of mixture [27]. Only the factors that have noticeable effects on assembly warpage are considered. The thickness of effective layer was the same as the height of the C4 bumps or the micro-bumps.

2.3. Warpage characterization and model validation

The warpage of FPGA package assembly in thermal cycling was measured via DIC method. The ramp rate of temperature is 10 °C/min and the temperature range is between 0 °C and 100 °C. Temperature dwell is 10 min. The warpage was extracted as the out-of-plane displacement on the diagonal of the measured area with respect to different temperature changes.

The three-step validation for the finite element model is illustrated in Figs. 8 and 9. In step 1, the metal lid was removed from the original 2.5D package, which is a lidless package in Fig. 8a. The warpage was measured on the substrate in the lidless package using DIC. The warpage data on the diagonal section was extracted. The relative warpages at 50 °C and 0 °C are plotted using 100 °C as the reference [28], which means the subtraction of the absolute warpage at 100 °C from the absolute warpage at 50 °C and 0 °C. The comparison between FEA results

Table 2
Material properties in finite element model.

Item	Young's modulus (GPa)	CTE (ppm/°C)	Poisson's ratio
PCB	See Fig. 5.		0.12
Substrate	See Fig. 6.		0.12
BGA (SAC305)	54	21.7	0.4
Die/interposer	170	2.5	0.36
Copper	110	16	0.343
C4 or μ-bump (63/37 SnPb)	32	24.7	0.38
Mold compound	16	8	0.3
Lid adhesive	0.072	200	0.4
Solder mask	2.4	43	0.25
Underfill in C4	8	75	0.3
Underfill in micro-bump	7.5	40	0.3

Table 3
Anand model parameters.

SAC 305 Anand model (ANSYS parameter)	Value	Unit
C1 (s_0)	12.4	MPa
C2 (Q/R)	9400	1/K
C3 (A)	4.00E+06	1/s
C4 (xi)	1.5	–
C5 (m)	0.303	–
C6 (h_0)	1378.952	MPa
C7 ($\hat{S}$)	13.78952	MPa
C8 (n)	0.07	–
C9 (a)	1.3	–

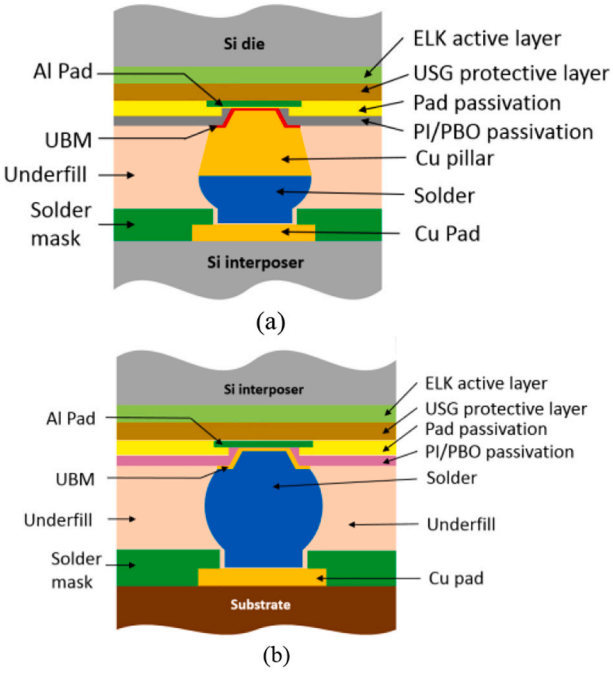

Fig. 7. Illustration of (a) microbump interconnect between silicon dies and silicon interposer, and (b) C4 interconnect between silicon interposer and organic substrate.

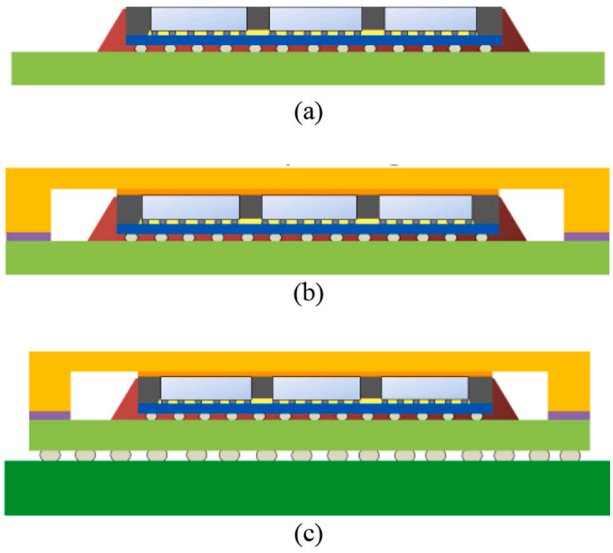

Fig. 8. Illustrations of packages in three-step validation for finite element modeling: a) step 1: lidless package, b) step 2: lidded package, c) step 3: assembly (package mounted on PCB).

and DIC measurement data is shown in Fig. 9a. In step 2, the 2.5D package with lid was measured. Similarly, the relative warpages of substrate obtained from FEA and measurement are plotted in Fig. 9b. In step 3, the package was mounted on a PCB and the relative warpages of PCB are plotted in Fig. 9c. The simulation results and measurement data reach good agreement. Via three-step validation high fidelity of the finite element model was provided.

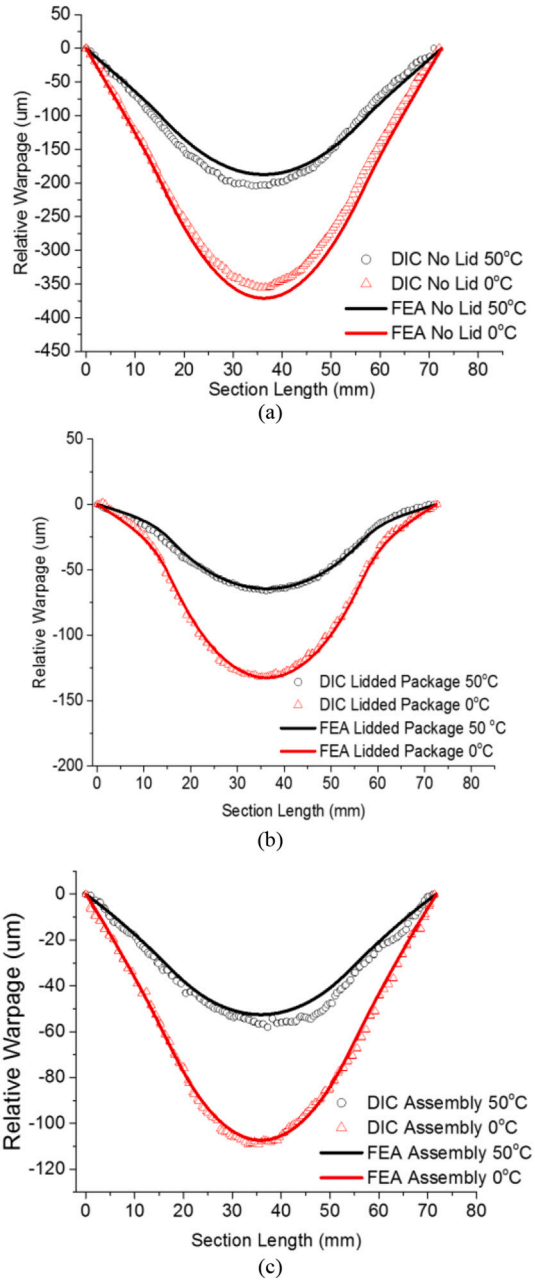

Fig. 9. Three-step validation of finite element model: a) step 1: substrate warpage of lidless package, b) step 2: substrate warpage of lidded package, c) step 3: PCB warpage of assembly. Absolute warpage at 100 °C is used to obtain the relative warpage.

3. Power cycling simulation

3.1. CFD model

A half-symmetry CFD model was established for conjugate heat transfer simulation. The CFD model is composed of fan, heat sink, FPGA package, and PCB. The FPGA package was molded with details, including thermal interface material (TIM), dies, interposer, substrate, solder joints, lid and lid adhesive. A unidirectional forced air flow is along Y axis with controlled velocities. Turbulent flow was solved within the cabinet. The environment temperature was 25 °C. Three dies

Table 4
Material properties in CFD model.

Item	Density (kg/m^3)	Specific heat (J/kg·K)	Conductivity (W/m·K)
Lid	8933	385	401
Die	2330	710	148
Substrate	1900	795	0.35
PCB	1250	1300	0.3
Solder	8690	239	56.9
Heat sink	2800	900	205
TIM 1& TIM2	1900	846	400 (in-plane); 6.5 (out-of-plane)

were powered in the package with 50 W per each. The duration of power on and power off is 5 min. The TIM2 thickness under heat sink was 2 mils (50.8 μm). The model had non-conformal mesh with hexahedra elements. The material properties are listed in Table 4. Fig. 10 shows the CFD model and the top/front view of mesh.

3.2. Data mapping from CFD model to finite element model

There are two aspects considered in data mapping from CFD to FEA, which are data storage methods and dissimilar meshes. Commercial software Fluent was used to solve CFD models, which is based on a finite volume method (FVM) approach. The variables (e.g. temperature) are stored at the centers of the mesh elements. On the other hand, variables are stored at nodes in finite element analysis. Cell centers (α_1, α_2, α_3, etc.) in FVM and nodes (1, 2, 3, etc.) in FEA are illustrated in Fig. 12. The purpose of temperature mapping is transferring temperature results from CFD models as body loads for finite element models, even though they have dissimilar meshes. Fig. 12 shows the mapping algorithm. The transfer variable is interpolated in sender side (CFD) first. The transfer values are obtained as

$$T = \phi(\alpha) \tag{1}$$

where ϕ is the interpolation function. Then, all nodes on the receiver side (FEA) query the sender side. Thus, each node in the finite element model acquires a mapping temperature from a cell in the CFD model. This process is realized by using ANSYS APDL coded scripts. A convenient way to execute the data mapping is to use an ANSYS Fluent FSI (Fluid-Structure-Interaction) module [29] with an APDL script. The APDL script is to export CFD results, call the FSI module and apply the loads on the nodes of the FE model.

Mapping quality was checked after transferring CFD temperature results to the corresponding nodes in the finite element model. Three paths are selected in the geometry. Path A is across the powered dies to represent the junction temperature. Path B is across the metal lid to represent the case temperature. Path C is across the PCB on its top side (solder joint side). Three paths are illustrated in Fig. 11b. CFD temperature results along the path are plotted as continuous lines, and their mapped temperatures are plotted as scattered data. Each mapped data point is the nodal temperature extracted from FE model to show whether the load transferring is done correctly. Fig. 13 shows that the nodal temperature loads in the finite element model match well with the CFD

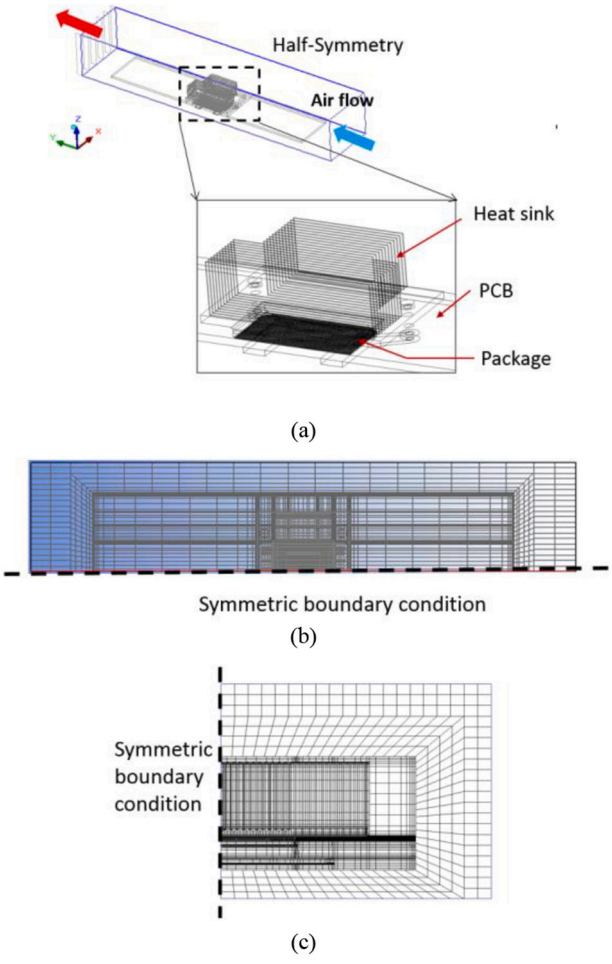

Fig. 10. CFD model of 2.5D package assembly for power cycling simulation. (a) CFD model with package, heatsink and PCB. (b) Mesh from top view (Z axis). (c) Mesh from front view (Y axis).

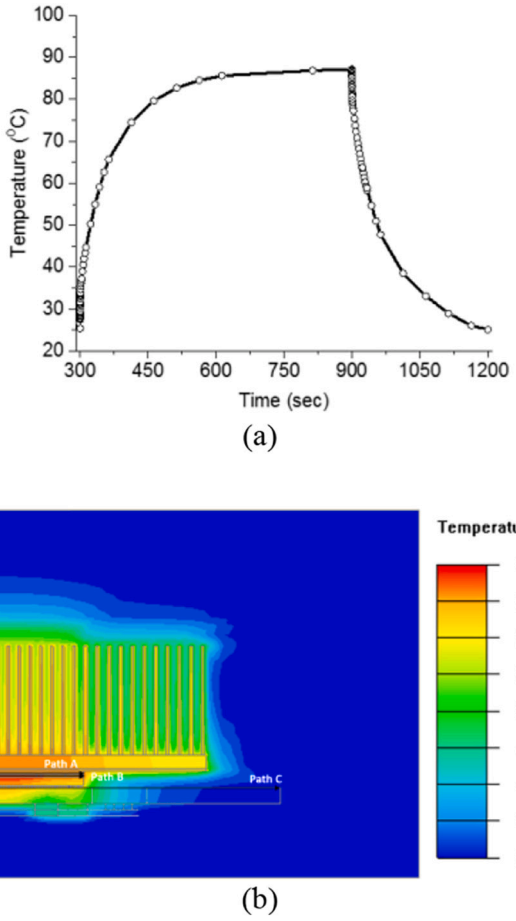

Fig. 11. CFD results of power cycling simulation. (a) Transient maximum junction temperature of package chip. (b) Temperature contour at t = 900 s. The cross section is normal to the air flow direction and through package center.

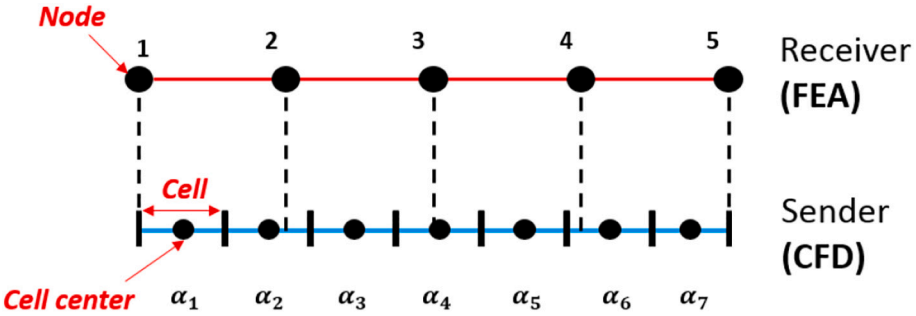

Fig. 12. Illustration of data mapping for dissimilar meshes from CFD to finite element model [29].

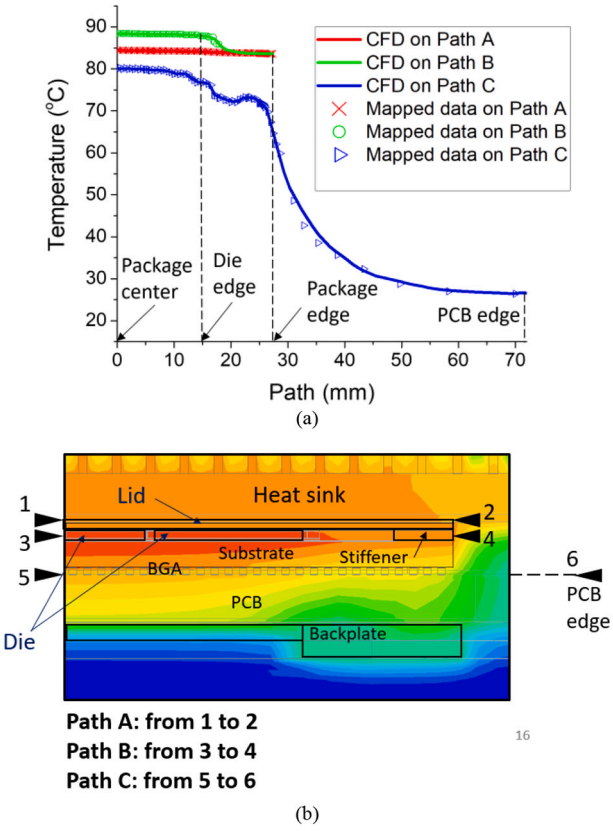

Fig. 13. (a) Comparison of temperatures along three paths between CFD results and mapped data on the nodes in the finite element model. (b) Three paths are illustrated. Path A is across the width of powered dies from the center to die edge. Path B is across the width of package lid. Path C is across the width on the top side of PCB.

results, proving an outstanding mapping quality.

There is one requirement to meet during applying the data mapping algorithm. The geometries of FE model are supposed to be the same or smaller compared to the CFD model in the same coordinate system [29], meaning the finite element model can be a part of CFD model. Therefore, it works for such a scenario where a CFD model has a liquid zone (air flow) and a solid zone (the 2.5D package assembly), and only the assembly is built for the finite element model.

A previously established methodology for power cycling simulation used transient heat transfer coefficients as surface loads to transfer into the finite element model [30], whose process flow is shown as Fig. 14a. The methodology using temperature mapping technique in this work is shown as Fig. 14b. Using the convective Heat Transfer Coefficient (HTC) for load transfer may need to divide the existing surfaces into smaller areas in the model, to capture high temperature gradients. Thus, simulation results may depend on the way of dividing surfaces. The advantage of using temperature mapping is that it can directly transfer the nonuniform temperature distribution from CFD to the finite element model. However, a potential data instability problem may exist. Since data interpolation takes part in the mapping, finer mesh in solid zone of CFD is usually needed to ensure the data stability.

4. Thermal cycling test

The thermal cycling test was performed following IPC-9701A standard [31]. The temperature range is between 0 °C and 100 °C, with 10-minute dwell time and 10 °C/min ramp rate. Event detector scanned continuously the daisy chain net for failure detection. The failure criteria were set as the resistance of the net beyond a threshold value (500 Ω), in a manner of 10-event occurrence and 1 microsecond duration for event detector. The test board was shown in Fig. 15. "Dye-and-Pry" technique was conducted to locate the failed BGA solder joint. One of the corner joints was found to have a fatigue crack. The optical image of its cross section was shown in Fig. 16. The crack was observed on the package side and it propagated inside the solder bulk. Two types of assemblies were tested. Twenty-six samples of lidded packages on PCB with no heatsink were tested having 9305 characteristic life cycles. Sixteen samples of lidless package on PCB with heat sink had 7027 characteristic life cycles. Here, heat sink was mounted in ATC test to study the effect of mounting force or clamping pressure on solder fatigue life.

5. Result and discussion

5.1. Solder fatigue life prediction

Syed [11] used a Coffin-Manson-type fatigue life model with a fitting constant for SAC alloy, the equation of which is shown as follows

$$N_f = (c\Delta W)^{-1} \tag{2}$$

where N_f is thermal cycles to failure, ΔW is accumulated inelastic work per volume per cycle in the critical solder joint, c is a fitting constant. This model presents the correlation between solder fatigue life and inelastic energy dissipation in the critical solder joint [32]. In this study, the constant c was determined using our own tested life data, besides the simulation result ΔW. In Table 5, ATC test life cycles of specimen 1, lidded package on PCB with no heat sink, was used to substitute N_f in Eq. (2). To obtain a proper value of ΔW without singularity, averaging method was adopted for a representative volume in the critical solder, the expression of which is shown as follows

$$\Delta W_{ave} = \frac{\sum (\Delta W_i \cdot V_i)}{\sum V_i} \tag{3}$$

The representative volume is shown in Fig. 17. Using the simulation methodology in Ref. [11], ΔW was computed and c was determined as 0.005646 (cycle·MPa)$^{-1}$, which was used to predict solder fatigue life for the board-level reliability life of 2.5D package assembly in both thermal cycling and power cycling in this work. Note that Anand

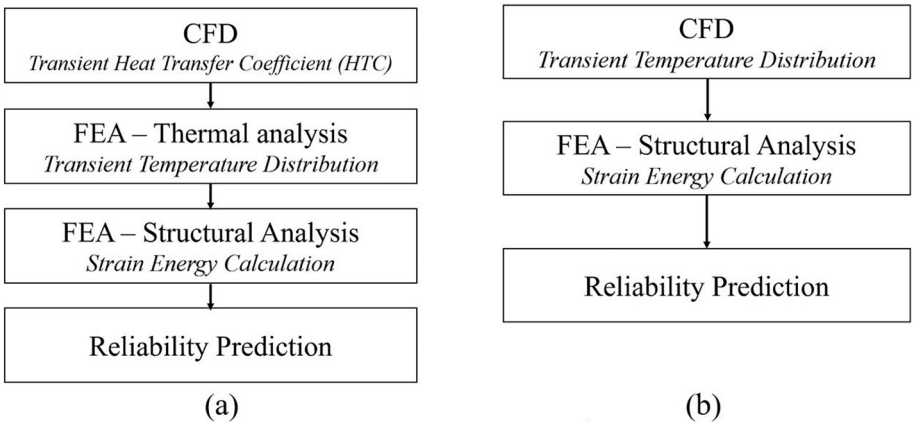

Fig. 14. Process flow charts for simulation methodology using (a) transient heat transfer coefficient for load transfer, and (b) transient temperature for load transfer.

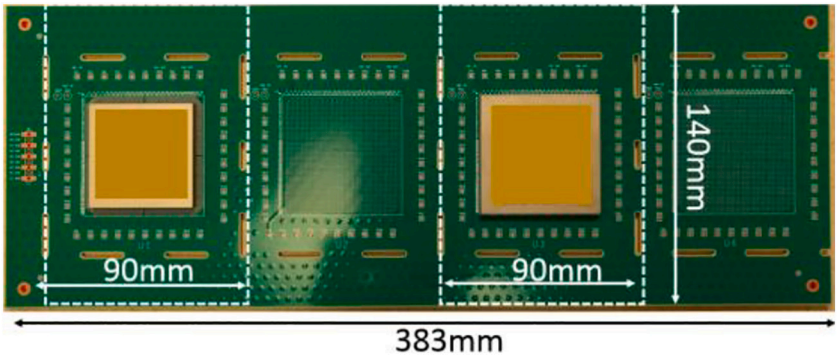

Fig. 15. Test specimen for board-level thermal cycling test.

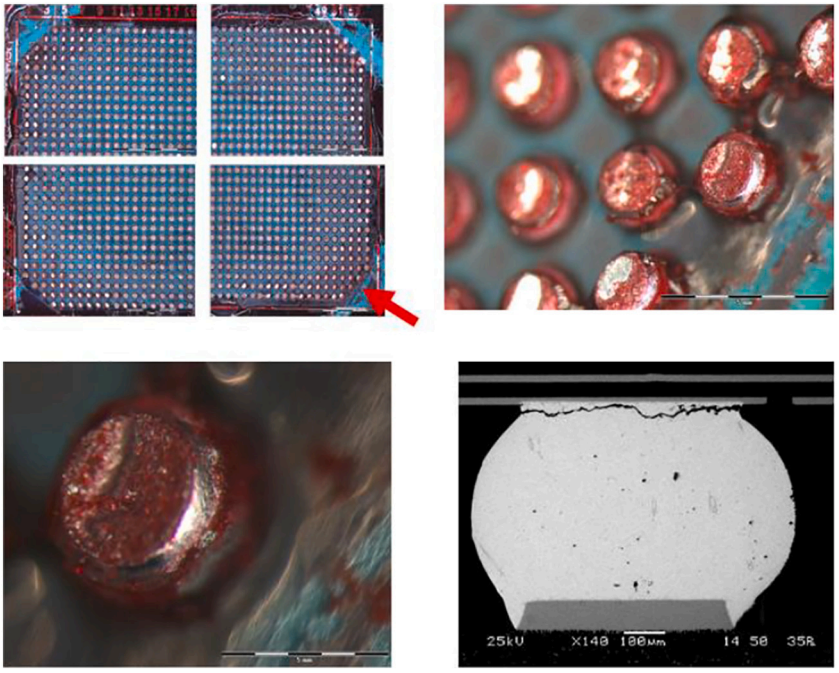

Fig. 16. Failure location of BGA in thermal cycling test and the optical image of the cross section of the failed corner solder joint.

Table 5
Tested life of 2.5D packages in board-level accelerated thermal cycling.

Test specimen for ATC	Sample amount	Tested thermal cycles to first failure	Predicted thermal cycles to first failure	Difference
1. Lidded package on PCB with no heat sink	26	8619	–	–
2. Lidless package on PCB with heat sink	16	5662	5614	0.86%

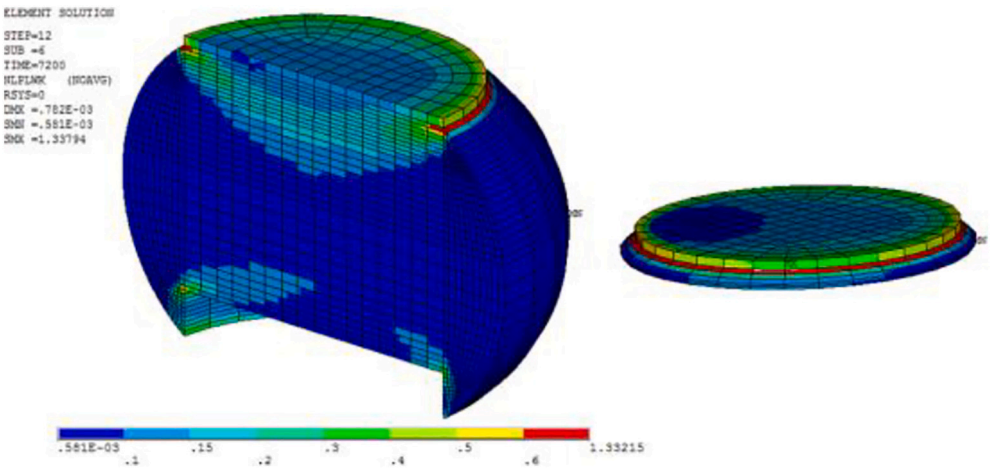

Fig. 17. Contour of inelastic work per volume in the corner solder joint after three thermal cycles from FEA results. A representative volume of solder is selected for averaging method, shown on the right.

Table 6
Parametric study variables for board-level reliability study.

	Unit	Value
Material variables		
Substrate CTE	ppm/°C	13.8, 16.5 (ref.), 19.3
Young's modulus of substrate	GPa	26.4, 33 (ref.), 40
PCB CTE	ppm/°C	15, 16.5, 17 (ref.), 18, 20
Young's modulus of PCB	GPa	14.4, 18 (ref.), 21.6
Metal lid CTE	ppm/°C	12, 14, 16 (ref.), 18, 20
Metal lid modulus	GPa	55, 85, 110 (ref.), 150, 220
Geometric variables		
Substrate thickness	mm	1.3, 1.8 (ref.), 2.1
PCB thickness	mm	2.4, 3.42 (ref.), 4.5
Metal lid thickness	mm	0.35, 0.5 (ref.), 0.65

*ref.: the reference value for normalization.

constitutive model was applied for SAC alloy in simulation. ΔW reached a stable status after three thermal cycles in simulation.

The tested life and the predicted life of test specimen 2, lidless package on board with heat sink, are listed in Table 5, with less than 1% deviation, showing that experiment data and simulation results match well. Statistically for fair comparison, the definition of first failure for both cases is that the first 5% of the population is failed. Compared to mean life or characteristic life, "first failure" life cycle has more practical meaning in perspective of product quality.

For simulating viscous materials such as solder, the stress status of solder is adjusted by the package structure during thermal cycling. The stress reaches the highest at the beginning of low temperature dwell and reaches the lowest at the end of high temperature dwell (stress relaxation). After enough times of cycling, the accumulated inelastic work per cycle in solder will reach a stabilized value, regardless of stress-free temperature. However, the amount of cycles needed to reach the stabilized value depends on the stress-free temperature. For example, it takes more cycles for ΔW to stabilize when the reflow temperature is used as the stress-free temperature, compared with the high temperature in thermal cycling. Usually high temperature in thermal cycling is used as the stress-free temperature to improve the computing efficiency, especially during running a case matrix to perform parametric study. Fan [33] compared three different stress-free temperatures: 1) high temperature from thermal cycling profile, 2) reflow temperature and 3) room temperature. The effect of changing stress-free temperature on simulation results of solder were analyzed, and the same conclusion was reached as this work.

5.2. Parametric study

Parametric study regarding material and geometry was performed to investigate their effects on solder fatigue life in accelerated thermal cycling. Parametric study variables are listed in Table 6 with respect to the substrate, the PCB and the metal lid. Note that all other factors remain when one single factor varies in this parametric study. ΔW was extracted from each simulation case and predicted fatigue life was obtained from Eq. (2). Fig. 18 shows the life prediction in the parametric study, where lives and material properties are normalized based on the reference cases in Table 6.

5.2.1. Effect of CTE of substrate and PCB

The effect of CTE on the fatigue life cycles is shown in Fig. 18. As the CTE of substrate increases, two trends of the fatigue life are found. For the substrate CTE lower than 17 ppm/°C, life becomes longer as substrate CTE increases. Then, the trend becomes opposite for the substrate CTE larger than 17 ppm/°C. Warpages of substrate and PCB are plotted in Fig. 19 as the substrate CTE varies, respectively. Their warpage difference is plotted in Fig. 20, subtracting the PCB warpage from the substrate warpage. The absolute values of the maximum warpage differences across the section length are denoted as z_1, z_2, z_3 and z_4. It is found $z_3 < z_2 < z_4 < z_1$ in Fig. 20, which is the same trend as the foregoing fatigue life. The warpage difference between substrate and PCB is directly related to the solder joint deformation. This result offers an insight of effect of substrate CTE.

On the other hand, solder stress and inelastic strain affect the inelastic work done in the solder joints, which is also involved in the

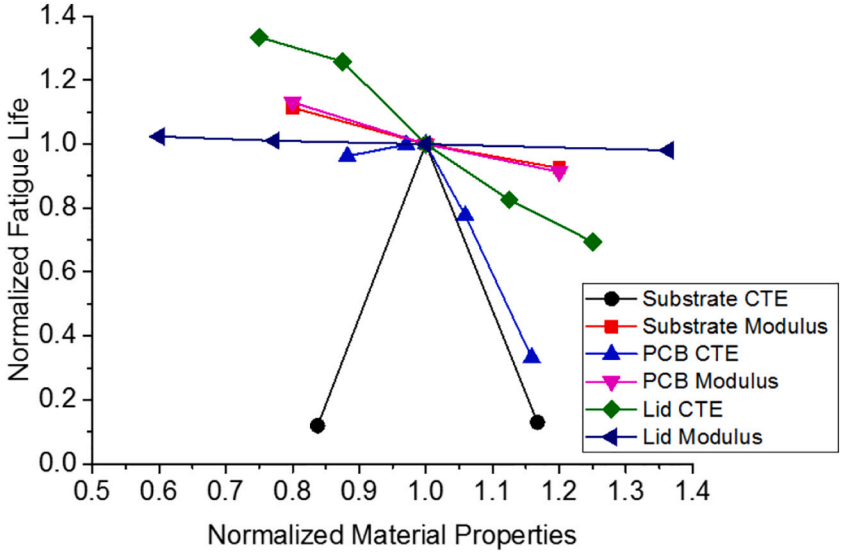

Fig. 18. Board-level fatigue life of the 2.5D package in thermal cycling regarding material properties of the substrate, PCB and metal lid. The variation of material properties and life predictions are normalized.

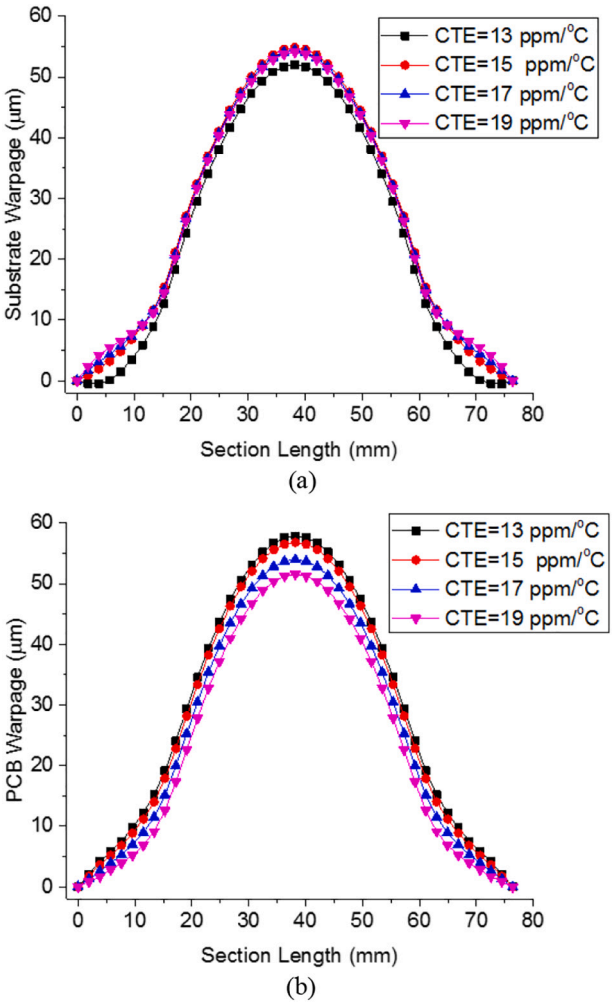

Fig. 19. Simulation results of relative warpages of (a) substrate and (b) PCB for various CTEs of the substrate in ATC. Reference temperature is 100 °C. Warpages are obtained at 0 °C.

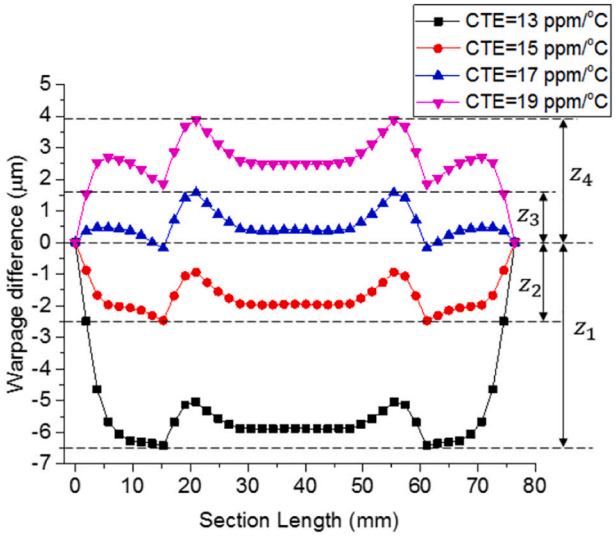

Fig. 20. Warpages difference of substrate and PCB for various CTEs of the substrate.

fatigue life. Equivalent creep strain and maximum Von Mises stress in the critical solder joint are plotted in Fig. 21, versus the substrate CTE variation. Normalization is based on the case where substrate CTE = 17 ppm/°C. The strains $\Delta\varepsilon_{creep}$ are the accumulated creep strains in one thermal cycle, with averaging in the representative volume that is the same as ΔW_{ave} calculation. It is evident that both the stress and the creep strain follow the same trend as the fatigue life versus substrate CTE, which provides another perspective on the effect of substrate CTE.

For the effect of PCB CTE, Fig. 18 shows that the fatigue life becomes shorter as PCB CTE is either lower than 16.5 ppm/°C or higher than 17 ppm/°C. Similar trends are found for the warpage difference, equivalent creep strain, and maximum Von Mises stress.

Both substrate CTE and PCB CTE significantly affect the fatigue life. Although different life trends occur for CTE above and below a certain value, a consistent trend is found when the factor of CTE mismatch between PCB and substrate is considered. The fatigue life becomes longer as the CTE mismatch decreases or becomes shorter as the CTE mismatch increases.

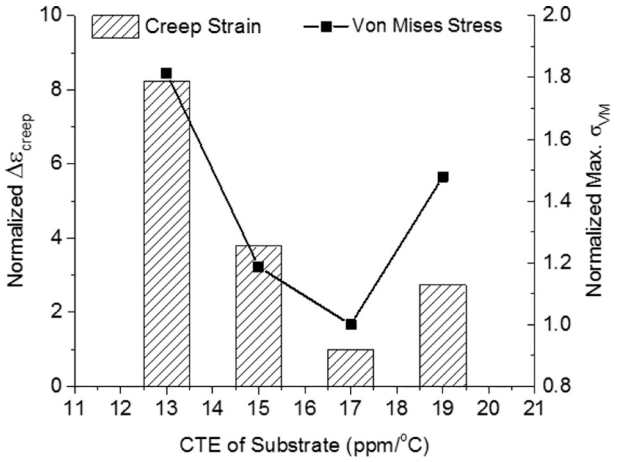

Fig. 21. Equivalent creep strain and maximum Von Mises stress of the critical solder joint for various CTEs of the substrate in ATC. Normalization is based on the case where substrate CTE = 17 ppm/°C.

5.2.2. *Effect of CTE of lid*

Fig. 18 shows the fatigue life becomes shorter as the CTE of the metal lid increases. The warpages of the substrate and PCB are obtained and plotted in Fig. 22. Interestingly, it is found that both substrate warpages and PCB warpage decrease as lid CTE increases, which is the opposite trend compared with fatigue life. The warpage shape tends to have a larger curvature at the edge of package. This phenomenon demonstrates the effect of the lid.

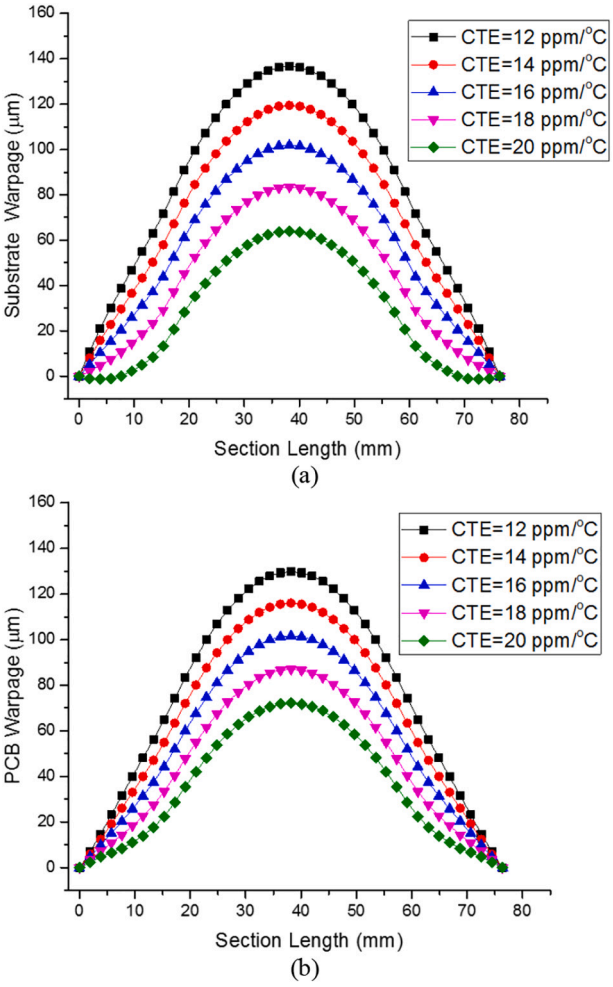

Fig. 22. Simulation results of relative warpages of (a) substrate and (b) PCB for various CTEs of the lid in ATC. Reference temperature is 100 °C. Warpages are obtained at 0 °C.

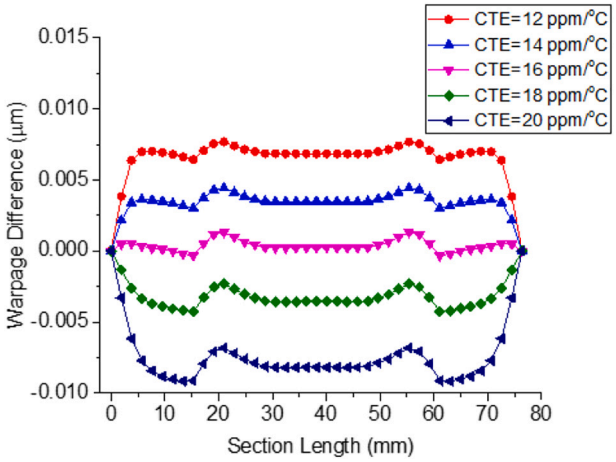

Fig. 23. Warpages difference of substrate and PCB for various CTEs of the lid.

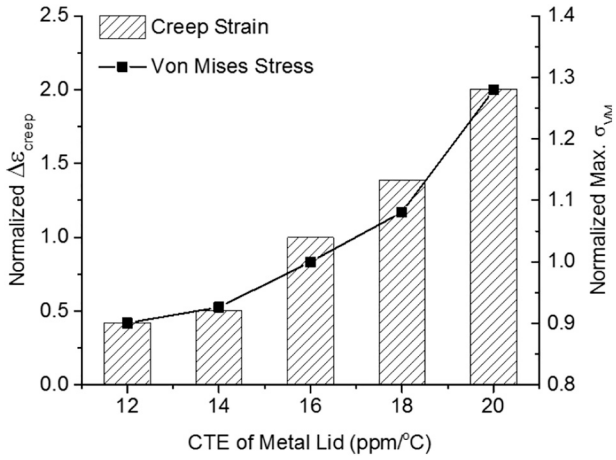

Fig. 24. Equivalent creep strain and maximum Von Mises stress in the critical solder joint for various CTEs of the metal lid in ATC. Normalization is based on the case where lid CTE = 16 ppm/°C.

The warpage difference is plotted in Fig. 23. However, it does not show the same trend as fatigue life. For example, the warpage difference with lid CTE = 16 ppm/°C is the lowest on in Fig. 23, instead of CTE = 12 ppm/°C.

The stress and the strain in the critical solder are plotted in Fig. 24. It is evident that both the stress and the creep strain increase as lid CTE increases in Fig. 24. The reason why the warpage difference shows a different trend with the equivalent strain and stress, is possibly that shear deformation of solder is not included in the warpage data.

5.2.3. *Effect of modulus of PCB, substrate and lid*

As the Young's modulus of substrate increases, the package itself becomes stiffer, as more deformations of the solder joints occur. Therefore, in Fig. 17, one can see life becomes shorter as the modulus of the substrate increases. It is the same reason that the same trend exists as PCB modulus increases.

There is very little change in life when lid modulus varies in Fig. 18. It is because the modulus is sufficiently large within the range of variation.

To rank the impact level and offer suggestions to improve manufacturing and service reliability, CTE mismatch between 2.5D package substrate and PCB exhibits the highest impact on board-level fatigue life

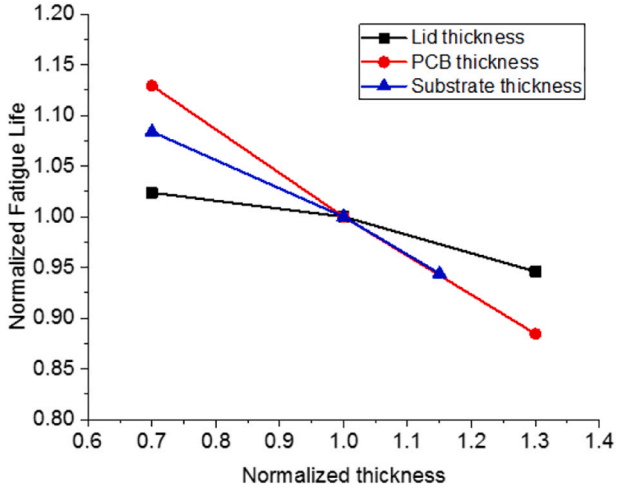

Fig. 25. Board-level fatigue life of the 2.5D package in thermal cycling regarding thickness of the substrate, PCB and metal lid. The variation of thickness and life predictions are normalized.

Table 7
CFD results of max. Junction temperatures at different inlet air flow speeds in power cycling.

Inlet air flow speed (m/s)	Max. junction temperature (°C)
1.3	115.9
1.5	105.5
1.7	97.7
2.0	89.3

in this parametric study. Lid CTE, the substrate modulus and the PCB modulus show less impacts. Lid modulus has a minimum influence on fatigue life.

5.2.4. Effect of thickness of PCB, substrate and lid

Fig. 25 shows the trends about the effect of thicknesses of the metal lid, the PCB, and the substrate, on the fatigue life cycles. Based on the classic plate theory, a larger thickness results in a larger flexure rigidity. This has the same impact on the deformation of the solder joints as increasing the modulus. Therefore, a smaller thickness of the lid, the PCB or the substrate is suggested to improve the board-level fatigue life of the 2.5D package.

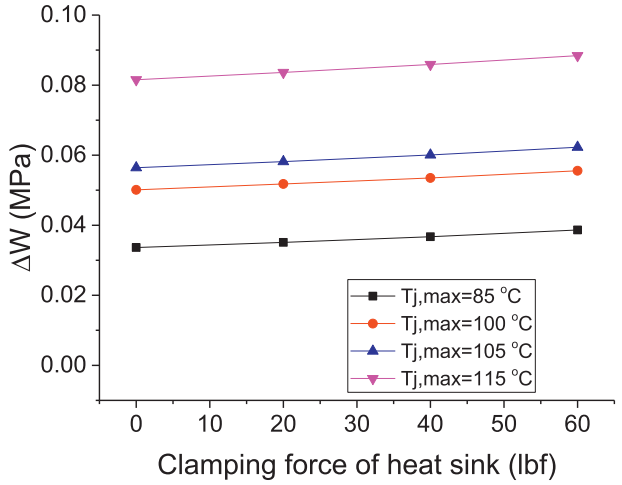

Fig. 26. FEA results of inelastic work ΔW versus heat sink clamping force for different maximum junction temperatures in power cycling.

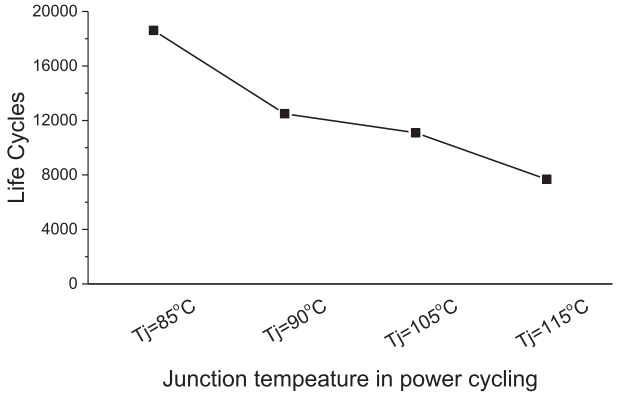

Fig. 27. Simulation results of solder fatigue life in power cycling under different maximum junction temperatures.

5.2.5. Effect of lid adhesive, TIM, microbump interconnect and C4 interconnect

Other factors are also considered for the parametric study. Using a much softer lid adhesive material with 50 times smaller modulus and 2 times larger CTE, solder life decreased by 10%. This is because copper lid alleviates the warpage of the assembly, thus improving lifetime in thermal cycling. A stiffer lid adhesive makes lid have a stronger impact on warpage. As the modulus of TIM1 changes by 50% and thickness of TIM1 changes by 50%, insignificant change in solder life was found from simulation results, assuming the same heat transfer performance and junction temperature. The same trend was found when underfill material properties change in C4 interconnect and micro-bump interconnect.

5.2.6. Junction temperature and clamping force of heatsink in power cycling simulation

Junction temperature changes as the chips switch on and off. The peak junction temperature is defined as the maximum value among all the chips in the package during the power cycling. Maximum junction temperature is related to the cooling air flow rate since larger air flow rate provides better cooling performance. Table 7 shows the maximum junction $T_{j,\ max}$ decreases as inlet air flow increases. The environment temperature of power cycling is 25 °C. Fig. 26 shows the effect of clamping force of heatsink on ΔW at each maximum junction temperature, which indicates that junction temperature has a significant impact on solder fatigue life in power cycling. Fig. 27 presents the corresponding solder fatigue life prediction in power cycling.

6. Conclusion

A design guideline for board-level reliability of 2.5D package was provided by FEA and CFD in this work. Finite element models were built for the bare package, the package with a lid, and the assembly. The warpage data between simulation and the DIC measurement reached good agreement. The inelastic work accumulation in the BGA solder joint under thermal cycling was computed, which is to be correlated with the tested fatigue life later to present a life projection model. CFD models were built to study the BGA reliability under power cycling. Data mapping from CFD model to finite element model was performed for a thermal-structure conjugate simulation. The data mapping method presented provides a more efficient way for such simulation, compared to the previous established method. Thermal cycling test was performed to obtain the actual board-level life data of the 2.5D package assemblies. Energy-based life projection model was adopted for board-level reliability analysis. The model constant in the Coffin-Manson-type life model was determined by correlating the thermal cycling life data and FEA results. Another set of tested life data were compared with the prediction from the life model and good

agreement was reached.

Furthermore, based on the correlated life projection model, a parametric study was performed aiming at providing 2.5D package design guideline for board-level reliability. Key material and geometry factors that affect board-level solder fatigue life were investigated, with regard to PCB, substrate, lid adhesive and TIM1. It was found that CTE mismatch between PCB and substrate is the major factor contributing to BGA fatigue life, instead of the PCB or the substrate solely. The fatigue life becomes longer as the CTE mismatch decreases or becomes shorter as the CTE mismatch increases. CTE mismatch between PCB and substrate should be minimized, to optimize the board-level reliability of 2.5D FPGA package. This finding is important because it requires package designers to consider not only the package components themselves, but also the related assembly process.

It was also found that both the stress and the inelastic strain increase as lid CTE increases. Lid CTE, the substrate modulus and the PCB modulus show less impacts. Lid modulus has a minimum influence on fatigue life.

A linear relation was found between the fatigue life and the thickness of lid, PCB, and substrate. A smaller thickness of the lid, the PCB or the substrate is suggested to improve the board-level fatigue life of the 2.5D package.

The modulus and the CTE of TIM1, C4 interconnect and micro-bump interconnect were found having minimal impact on BGA fatigue life in this study.

For board-level reliability in power cycling, it was found that the designed maximum junction temperature has a considerable influence, while the applied heatsink clamping force has much less.

7. Future work

Utilizing the assessment method presented in this study, more investigate can be conducted in the future. With a different temperature range of thermal cycling, the conclusion for solder joint reliability could be different because the glass transition temperature of substrate and PCB may have to be considered. By including the variation of packaging technology, BGA solder material and geometry in the study, an alternative life projection model with a wider range of application could be achieved.

Credit author statement

Shuai Shao: Writing - Original Draft, Conceptualization, Methodology, Formal analysis, Visualization. **Yuling Niu**: Conceptualization, Methodology, Validation, Writing - Review & Editing. **Jing Wang**: Conceptualization, Methodology, Validation, Writing - Review & Editing. **Ruiyang Liu:** Conceptualization, Methodology, Validation. **Seungbae Park**: Supervision, Project administration, Conceptualization, Methodology. **Hohyung Lee**: Resources, Data Curation. **Laurene Yip**: Resources, Data Curation. **Gamal Refai-Ahmed**: Supervision, Project administration.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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