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# Stress analysis of a novel MEMS microphone chip using Finite Element Analysis

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## ABSTRACT

Residual stress produces major challenges in the fabrication of MEMS devices. This is particularly true in the development of MEMS microphones since the response of the thin sound-sensitive diaphragm is strongly affected by stress. It is important to predict the effects of fabrication stress on the microphone chip and identify the failure modes to ensure a satisfactory fabrication yield. In this study, a finite element model of the microphone chip is developed to analyze the laminated structure under different fabrication stresses. The model of the microphone chip includes the diaphragm, backplate and sacrificial oxide layers on top of the silicon substrate. Fabrication stresses are included through the use of an equivalent thermal stress. The stresses in the different layers have been estimated based on measurements performed on fabricated test structures. The estimated stresses are simulated in the finite element model. An important factor in determining the process reliability is the compressive stress of the low temperature sacrificial oxide layer (LTO). A variety of stress combinations between different layers with the low temperature oxide layer are investigated. It is found that an adequate level of tensile stress in the backplate is crucial to ensure the fabrication yield. In the designs considered here, silicon nitride in combination with a thin conductive layer is identified as a favorable material for the backplate considering its high modulus and tensile stress in 'as deposited' film. In addition, the presence of a LTO layer on the backside of the wafer turns out to be very helpful in reducing the deflection of the unreleased chip and the stress in the diaphragm. In the case where there is a net compressive stress in the laminate, the failure mode is identified by nonlinear analysis. This analysis provides a guideline to select robust materials and tune the fabrication process to ensure a satisfactory fabrication yield.

## INTRODUCTION

Residual stress produces major challenges in the fabrication of MEMS devices. This is particularly true in the development of MEMS microphones since the response of the thin sound-sensitive diaphragm is strongly affected by stress. It is important to predict the effects of fabrication stress on the microphone chip and identify the failure modes to ensure a satisfactory fabrication yield. In this study, a finite element model of the microphone chip is developed to analyze the laminated structure under different fabrication stresses. The model of the microphone chip includes the diaphragm, backplate and sacrificial oxide layers on top of the silicon substrate. Fabrication stresses are included through the use of an equivalent thermal stress. The stresses in the different layers have been estimated based on measurements performed on fabricated test structures. The estimated stresses are simulated in the finite element model. An important factor in determining the process reliability is the compressive stress of the low temperature sacrificial oxide layer (LTO). A variety of stress combinations between different layers with the low temperature oxide layer are investigated. It is found that an adequate level of tensile stress in the backplate is crucial to ensure the fabrication yield. In the designs considered here, silicon nitride in combination with a thin conductive layer is identified as a favorable material for the backplate considering its high modulus and tensile stress in 'as deposited' film. In addition, the presence of a LTO layer on the backside of the wafer turns out to be very helpful in reducing the deflection of the unreleased chip and the stress in the diaphragm. In the case where there is a net compressive stress in the laminate, the failure mode is identified by nonlinear analysis. This analysis provides a guideline to select robust materials and tune the fabrication process to ensure a satisfactory fabrication yield.

## 2. FEA model

Figure 1 illustrates the 7-mask fabrication process used for this silicon microphone design.

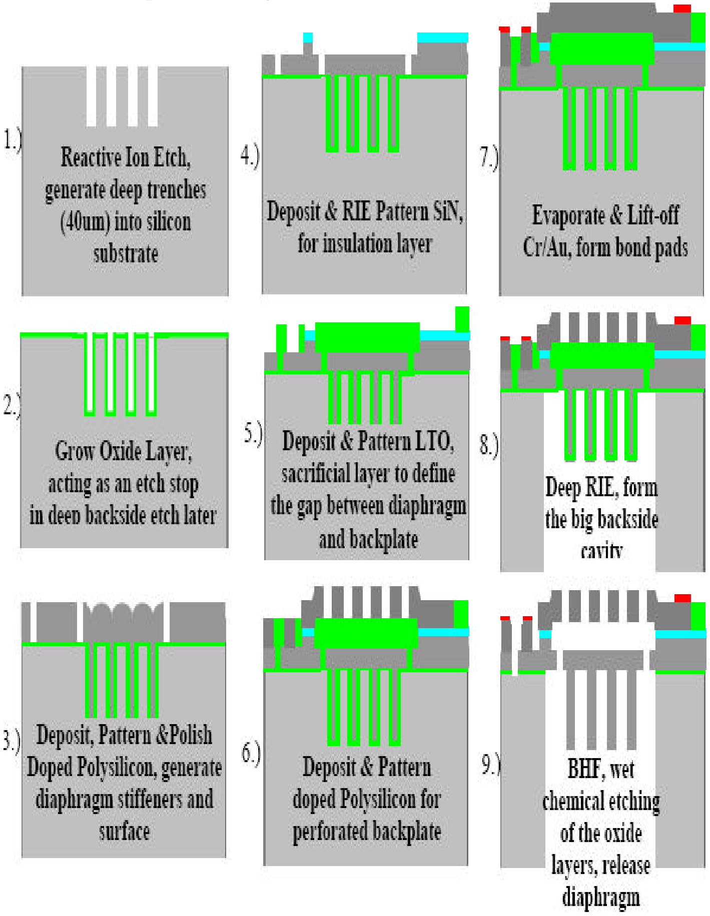

Figure 1 Fabrication process flow of a silicon microphone

A detailed FEA model of the microphone chip is completed in order to investigate the deflection of the entire laminate structure of the microphone chip due to fabrication stress. The modeled microphone chip includes different thin film layers stacked on top of each other. The stacking sequence is: 4 micron thick in-situ phosphorous doped polysilicon backplate, 5 micron thick low temperature oxide (LTO) to form the gap between the diaphragm and the backplate, 2 micron thick in-situ phosphorous doped polysilicon diaphragm, and 385 microns thick single crystal silicon substrate. The stresses in the different layers have been identified by various test methods on fabricated test structures. The diaphragm layer has a slightly tensile stress. The LTO and backplate layers have approximately 200 and 100 MPa compressive stress respectively. Figure 2 shows the modeled fabrication process step illustrated in figure 1, step 8. Figure 3 shows the stacking sequence of FEA model.

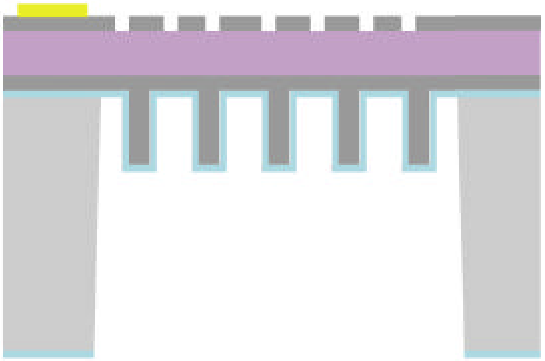

Fig.2 Modeled fabrication process step

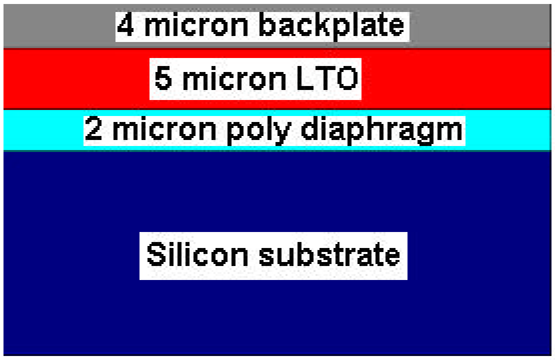

Fig.3 FEA model schematic

Figure 4 shows the SEM image of the fabricated microphone chip. Figure 5 is the FEA model representation.

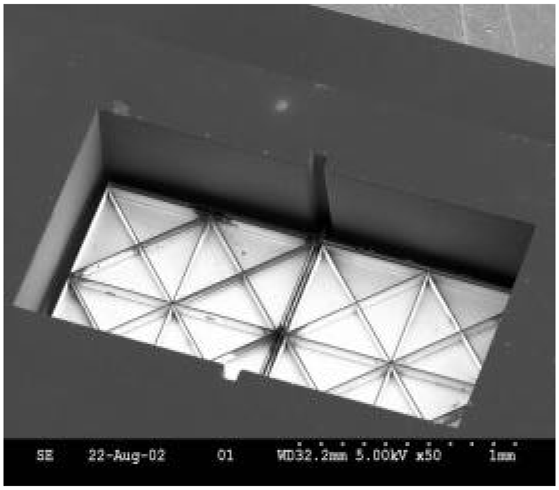

Fig.4 SEM image of microphone chip

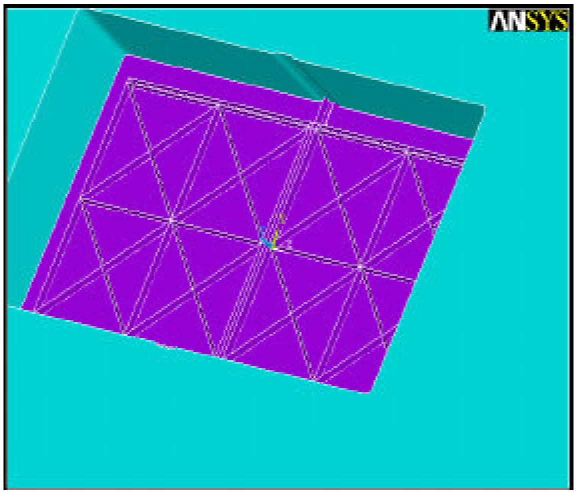

Fig.5 FEA model of laminated microphone chip

Figures 6 and 7 show the close up plots of the different layers.

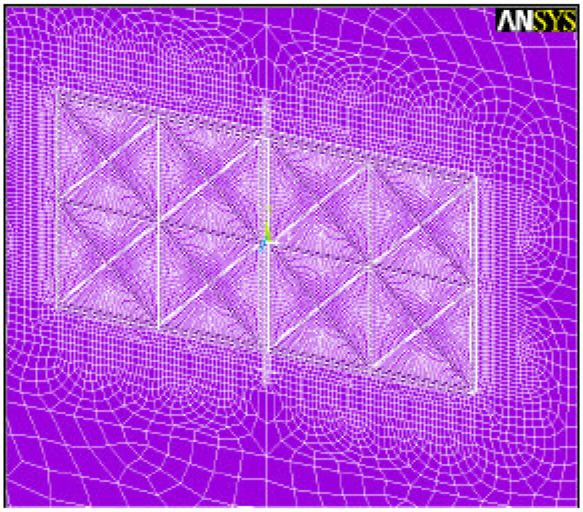

Fig.6 Diaphragm element plot

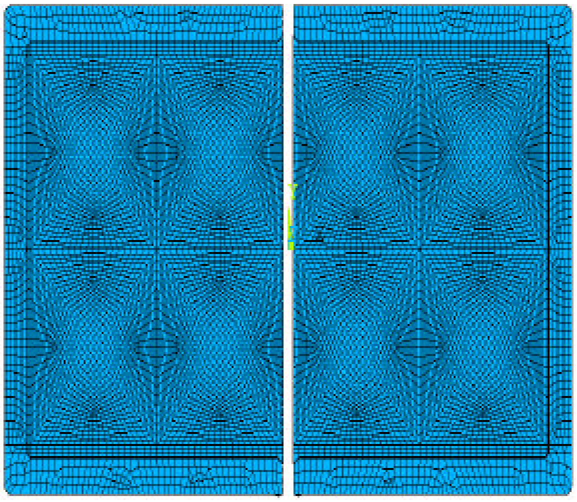

Fig.7 Backplate element plot

The acoustic holes in backplate are neglected to simplify the FEA model. In practice, the backplate is highly perforated to create the desired acoustic damping and finally release the structure from sacrifical oxide layer below the backplate.

Analyses have been completed that assume a polysilicon backplate with either compressive or tensile stress as well as a silicon nitride backplate with tensile stress. The stress in the polysilicon diaphragm and LTO remain the same as mentioned above.

### 2.1 Polysilicon backplate with a 100 MPa compressive stress

Figures 8 to 18 show the results for the polysilicon backplate with 100 MPa compressive stress.

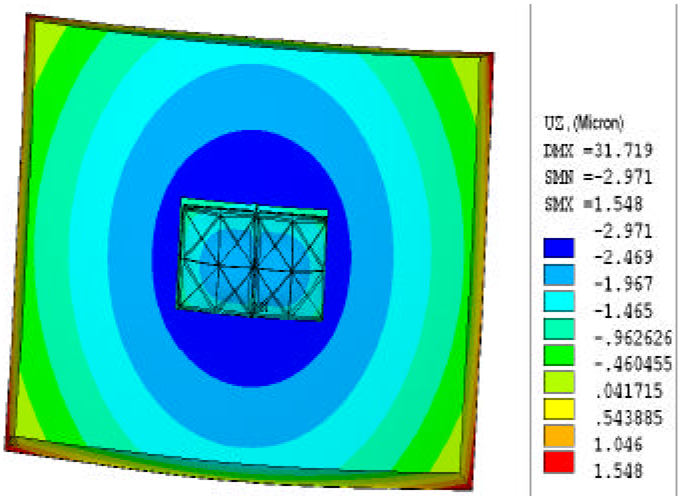

Fig. 8 Deflection of microphone chip

It is shown that the deflection of the microphone chip is about 4.5 micron before releasing the 5-micron LTO layer in order to leave the 5- micron gap between the diaphragm and the backplate. Based on this result, the deflection is not likely to cause failure of the structure. But it may introduce other fabrication issues during the finally release of the device. So, it is essential to keep the deflection of microphone chip as low as possible in order to maintain the structural integrity of the devices throughout the fabrication process.

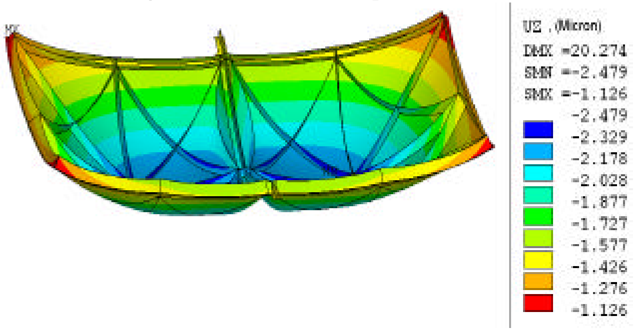

Fig.9 Deflection of diaphragm (exaggerated view)

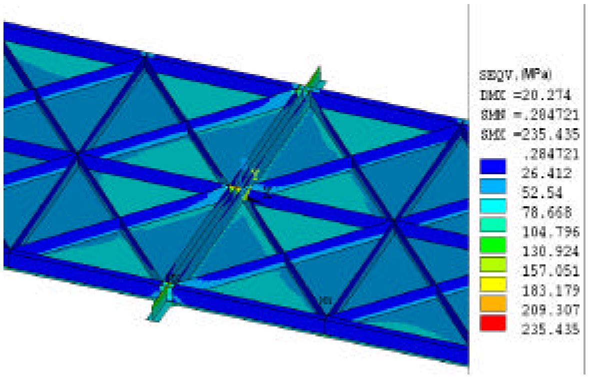

Fig.10 von- Mises stress of diaphragm

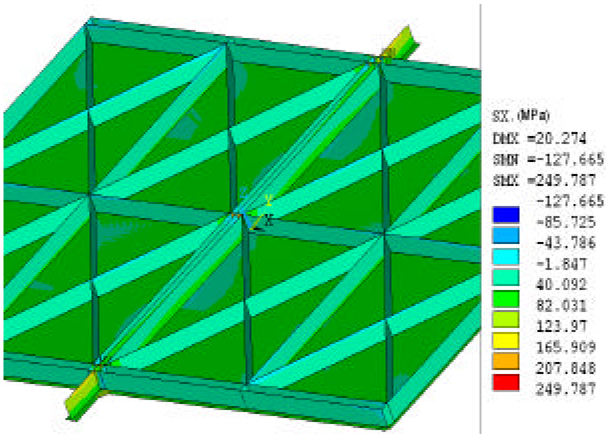

Fig.11 x-dir stress of diaphragm

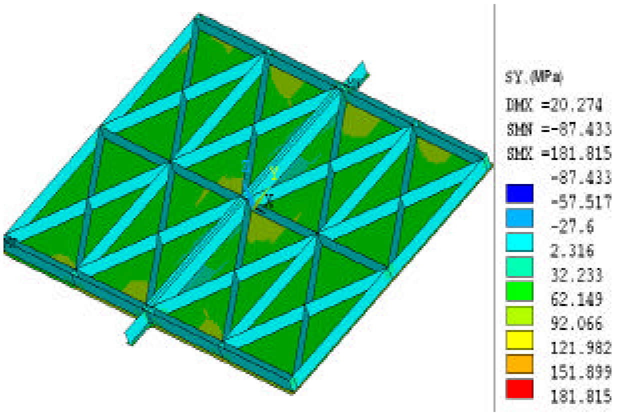

Fig.12 y-dir stress of diaphragm

The results indicate that the stress concentration in the diaphragm should be in the safe range.

It should be noted that polysilicon and bulk silicon are brittle materials, and therefore typically do not yield before failure. Although von-Mises is the failure criteria valid primarily for ductile materials, it is used through the analyses to acquire the information about the multi-axial state of stress. It is used for overall stress estimation rather than the failure criteria.

Figures 13 and 14 show 200 MPa compressive stress in the LTO layer.

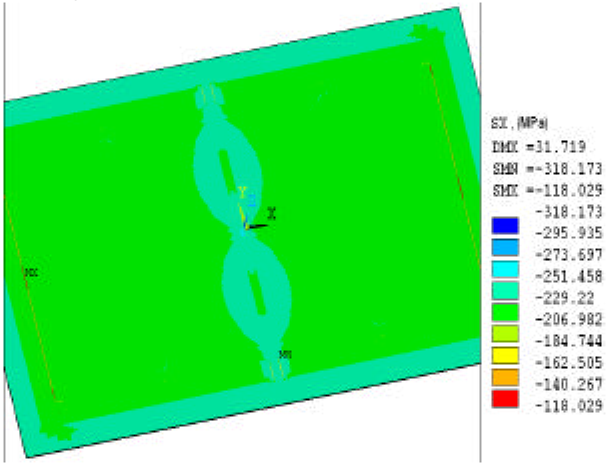

Fig.13 x-dir stress of LTO

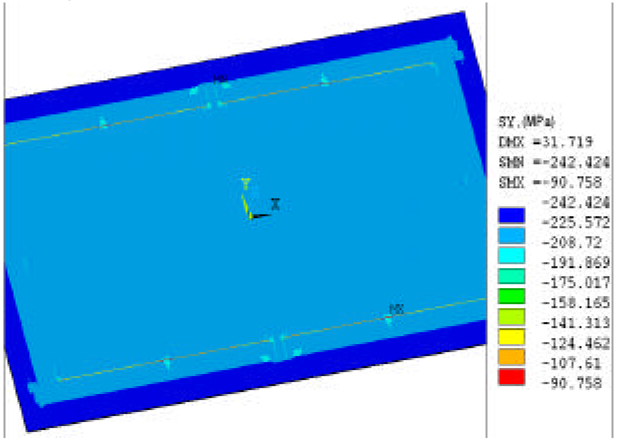

Fig.14 y-dir stress of LTO

Figures 15 and 16 show stress results in the backplate layer.

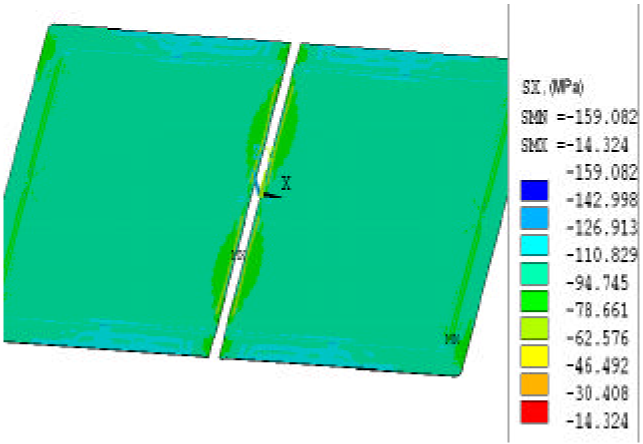

Fig.15 x-dir stress of poly backplate

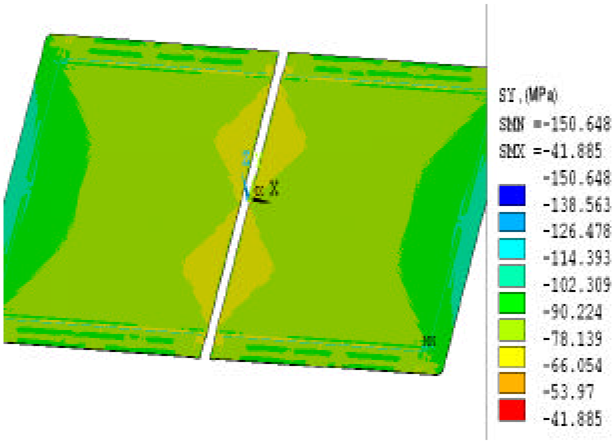

Fig.16 y-dir stress of poly backplate

It is found that the stress in the polysilicon backplate is around 100 MPa compressive, indicating that stress concentrations do not play a significant role.

### 2.2 Polysilicon backplate with slight tensile stress

Figures 17 to 25 show the results for the polysilicon backplate with a small amount of tensile stress.

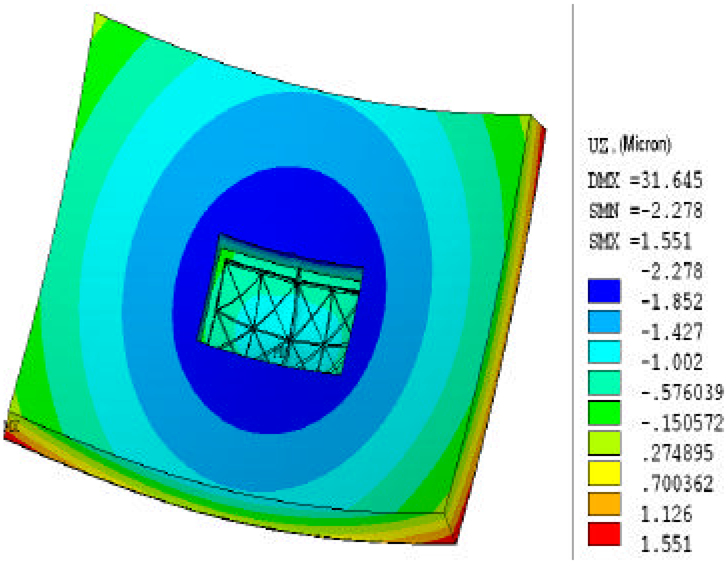

Fig.17 Deflection of microphone chip

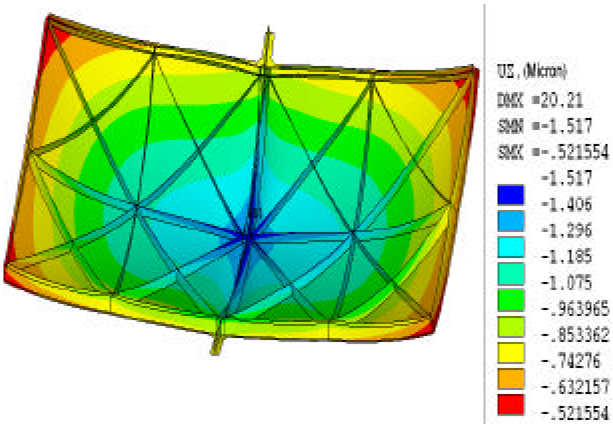

Fig.18 Deflection of diaphragm

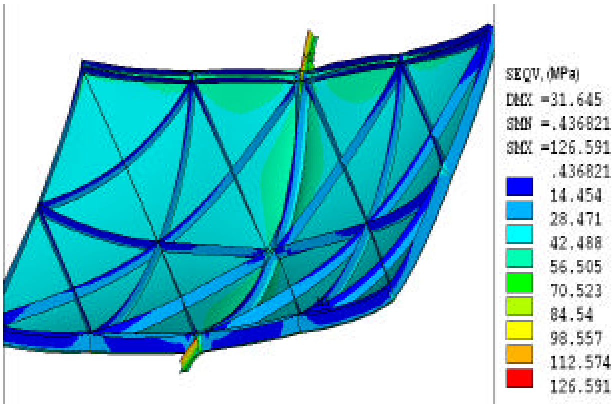

Fig.19 von-Mises stress of diaphragm

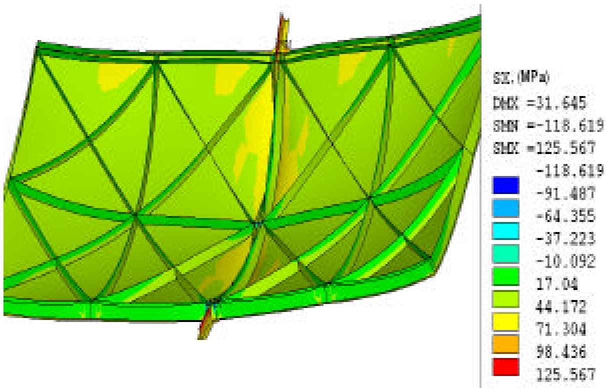

Fig.20 x-dir stress of diaphragm

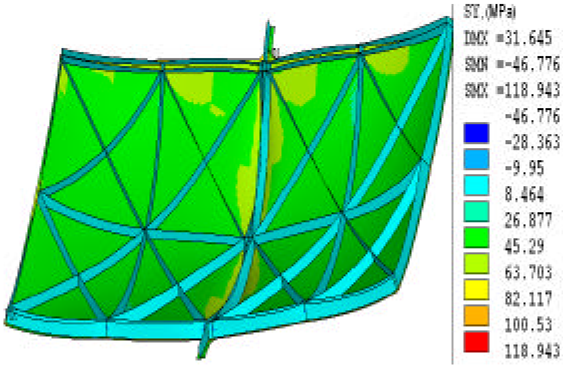

Fig.21 y-dir stress of diaphragm

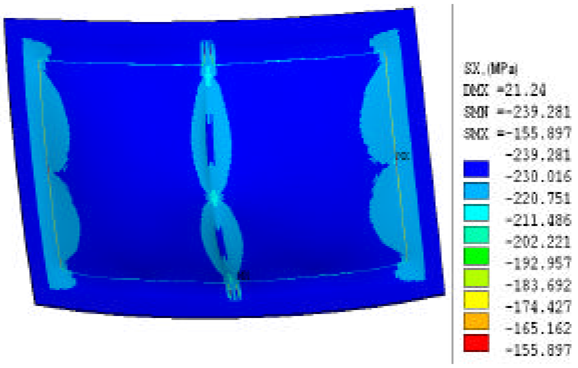

Fig.22 x-dir stress of LTO

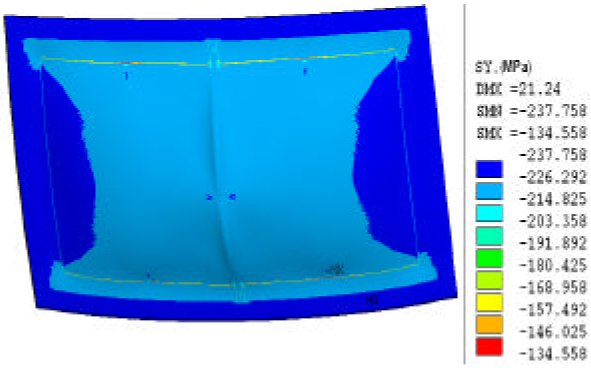

Fig.23 y-dir stress of LTO

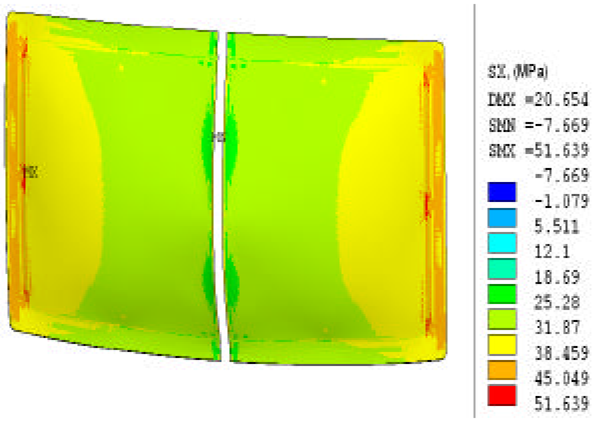

Fig.24 x-dir stress of poly backplate

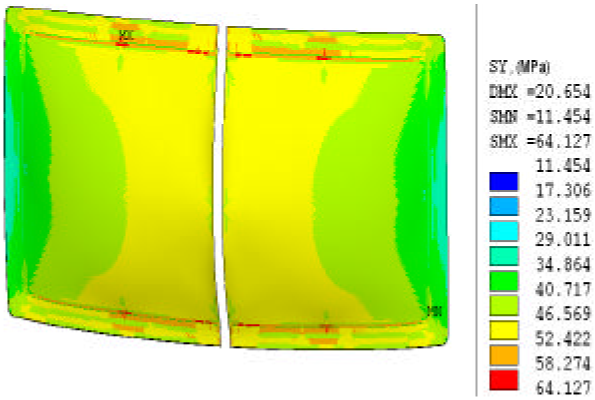

Fig.25 y-dir stress of poly backplate

In this case, the poly backplate is simulated to have a slightly tensile stress. The stress in the LTO remains the same as in case 1.

### 2.3 Additional LTO layer on the backside of the silicon wafer with a slightly tensile stress in the polysilicon backplate

Analysis has also been completed for the instance when the LTO layer remains on the backside of the silicon wafer. The stress in the polysilicon backplate is assumed slightly tensile. Figures 26 and 27 show the FEA model and schematic of layers stacking sequence.

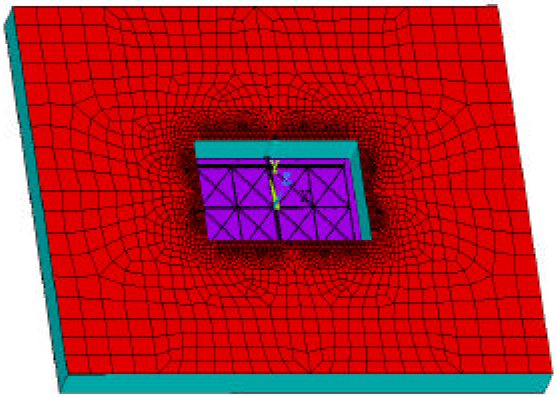

Fig.26 FEA model

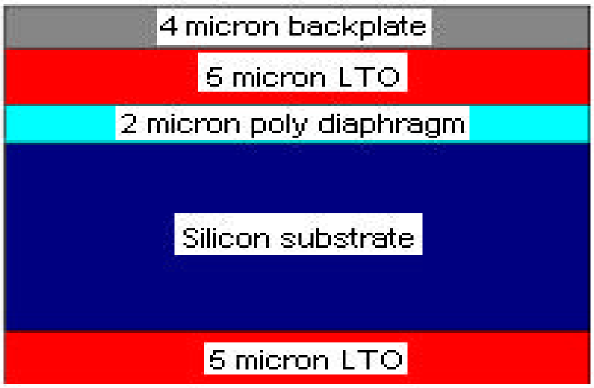

Fig.27 Schematic, LTO layer on backside of wafer

The results for the different cases are summarized in table 1.

| | Case 1 Poly-backplate Stress, -100Mpa | Case 2 Poly backplate Stress, slightly tensile | Case 3 Nitride-backplate Stress, 200MPa | Case 4 Poly-backplate Stress, slightly tensile, LTO layer backside of wafer |
|---|---|---|---|---|
| Microphone chip deflection | 4.5 micron | 3.8 micron | 3.3 micron | 2.2 micron |
| Stress in LTO layer | -200 MPa | -200 MPa | -200 MPa | -200MPa |
| Maximum diaphragm deflection | 1.4 micron | 1 micron | 1 micron | 0.7 micron |
| Maximum stress in diaphragm (in-plane) | 250 MPa | 125 MPa | 145 MPa | 112 MPa |
| Maximum backplate deflection | 1.3 micron | 0.9 micron | 0.9 micron | 0.6 micron |

Table 1 Summary of results for four cases simulated

Based on these results, it can be concluded that none of the investigated stress configurations would lead to the structure failures although the case of poly-backplate with compressive stress leads to the largest deflection of microphone chip as well as the highest stress in diaphragm. The additional LTO layer remaining on the backside of wafer is helpful in reducing the microphone chip deflection and the stress in the diaphragm. It is then suggested that this LTO layer on backside of the wafer should be kept in place until the final release of the device.

It is important to note that all these results presented above are based on a linear analysis that assumes a linear relation between loading and deflection. It may neglect the failure mode related to the instability of the laminate under a net compressive loading caused by specific stress combinations between the different layers. To properly complete the stress analysis of the microphone chip, a nonlinear static analysis is used to investigate the instability of the laminate due to the net compressive loading caused by the stress combinations specified in case 1 in Table1.

### 2.4 Nonlinear analysis of polysilicon backplate with 100 MPa compressive stress

Figures 28 to 30 show the nonlinear analysis results of the microphone chip in the case of polysilicon backplate with a 100 MPa compressive stress. The stress in LTO layer is assumed to be 200 MPa compressive.

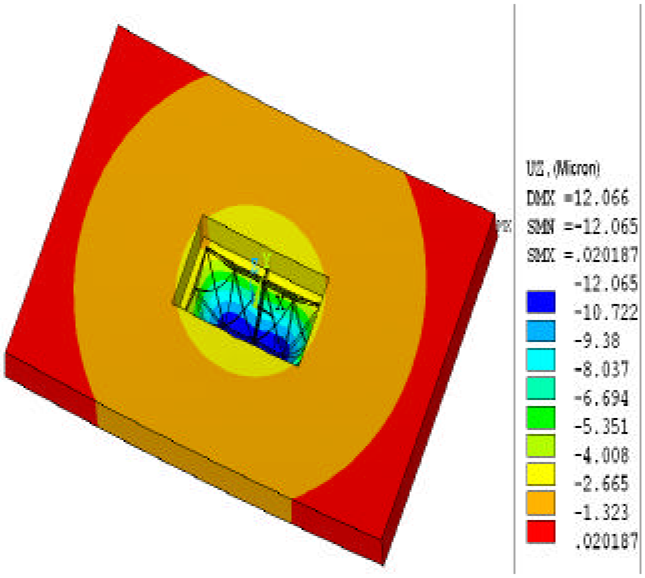

Fig.28 Deflection of microphone chip

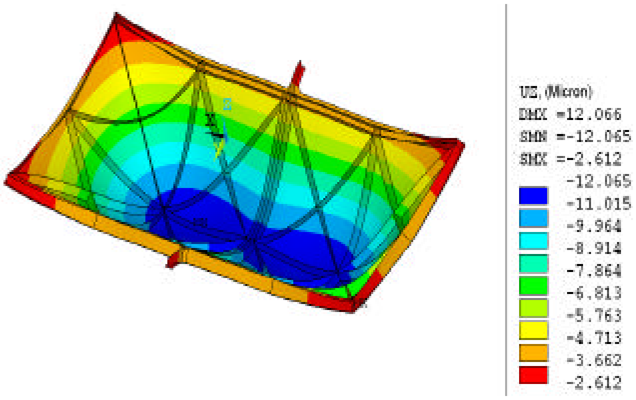

Fig.29 Deflection of diaphragm

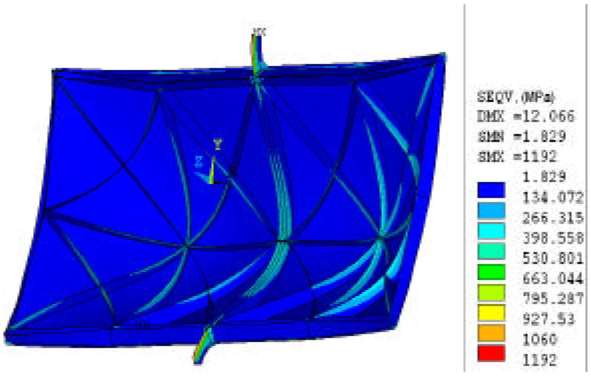

Fig.30 von mises stress of diaphragm

The results from this stress analysis show that with the compressive stress in the LTO layer, the compressively stressed polysilicon backplate will have the largest deflection of the chip and stress in the diaphragm. The LTO layer remaining on the backside of the silicon wafer will effectively reduce the deflection of the microphone chip as well as stress in the diaphragm. In the case where there is a net compressive stress in the laminate, the deflection of the microphone chip is above 12 microns and the maximum stress is about 1.2 GPa at the diaphragm supports based on this nonlinear analysis. Such a large deflection and stress will cause the failure of microphone chip. The failure mode is thus identified by nonlinear analysis, which provides a good explanation for the catastrophic deflection of the microphone chip observed during fabrication. It should be pointed out that the analyses have been done for the microphone chip, which has not been completely released. The loading from the LTO layer underneath the backplate will be mostly released after the LTO layer is etched away. Most of the elastic deformation of the backplate due to the loading of compressive stress in the LTO will be recovered. The final deflection of the backplate will primarily depend on the stress state of the backplate itself. In the case of compressive stress, the backplate may be buckled if the stress is too much. If the stress is highly tensile, the cracks may be generated and propagate which would break the backplate considering the high stress concentration in the highly perforated backplate design. In the case of compressive stress in the backplate, it is crucial to predict the critical buckling loading in order to avoid fabrication failure for the fully released device. The critical buckling loading predicted by nonlinear FEA analysis is shown in figures 31 and 32.

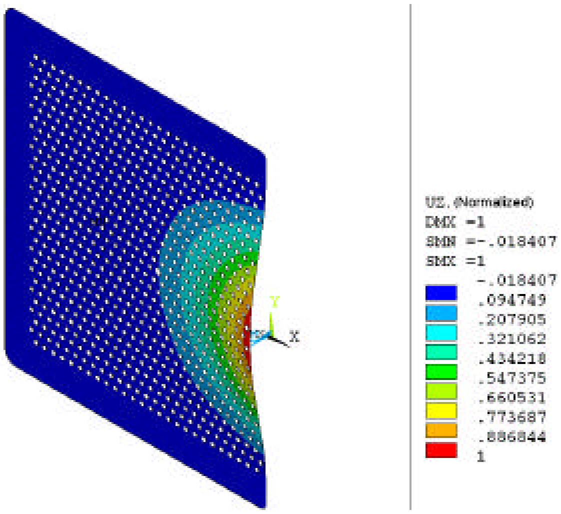

Figure 31 First buckling shape

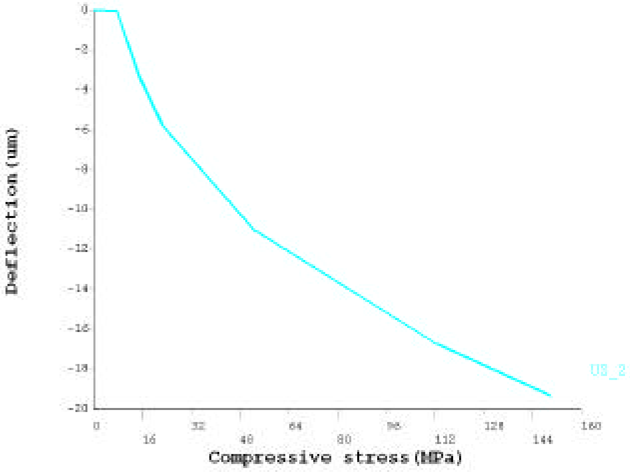

Figure 32 Loading - deflection curve by nonlinear analysis

From the loading and deflection curve shown in figure 32, the first critical buckling load for the poly backplate is approximately 10 MPa of compressive stress. By the stress identified from the current process for the poly backplate, the 'as deposited' stress is typically in the order of hundreds of MPa compressive, which is far above its critical buckling loading. Therefore, the chances of the backplate with compressive stress surviving the final release are very low. Based on all these analyses, it is very clear that tensile stress in the backplate is crucial to ensure a fabrication yield. Silicon nitride should be a favorable material for the backplate considering its high modulus and tensile stress in 'as deposited' film. However, efforts should be made to keep the tensile stress in a range below 200~300 MPa in order to avoid crack generation and propagation due to the high stress concentration at the acoustic holes in the backplate. The LTO layer on the backside of the wafer turns out to be very helpful to reduce the deflection of the unreleased microphone chip and the stress in the diaphragm. It is beneficial to keep it on the wafer until the final release of the microphone chip.

## ACKNOWLEDGMENTS

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